

Integrated Circuits

FOXBORO







FOXBORO INTEGRATED CIRCUITS

SK. 19227

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The Foxboro Company Foxboro, Massachusetts 02035

HISTORY

Version	Date	Copies	Remarks
A	10/73	200	Original edition

PREFACE

This book (document 73002BZ) is intended as an aid to maintenance personnel servicing process management and control equipment such as FOX 2 Systems. It contains information necessary to trace signals through or replace integrated circuits (ICs). ICs described herein are used in standard system components manufactured by The Foxboro Company. ICs in standard system components, such as computers, drums, CRT consoles, etc. that are part of the Foxboro product line, but not manufactured by The Foxboro Company, are not included.

Foxboro part numbers and equivalent IC manufacturer's part numbers are identified in Table 1. This table can be used as a parts substitution list in the replacement of integrated circuits.

All integrated circuits described in this standard book might not be in any given system, and any ICs for custom modules designed specifically for your system are not covered in this standard book.

IC information is presented in Foxboro part number sequence, as indicated in the table of contents. Pages are not numbered, so information on an IC is located relative to the alpha-numeric part number sequence.

Table 1. Integrated Circuit Cross Reference Oata

FOXBORO	Τ	N.S.C	SPRAGUE	MOTOROLA	FAIRCHILO	0EC	SIGNETICS
C3002RR	NOT 151 NON						
C3004NS	SN75107N						
C3004NT	SN7403N	DM8003M	USN7403				
C3004NW	SN7404W	0M8004N	USR:7404	MC7404P			
C3004PL	SN74121						
C3007MR	SN7405N		USN7405A	MC7405P			
C30088Z	SN74107						
C3008FL	SM7442						
C3009SH					8083		
C300955					6366		
C30095T							481018
C3313AA						380A	
C3313AB						8881	
C3313AC	SN7407						
C3313A0	SN74H78-N-						
C3313AE	SN7486-N						

Table 1. Integrated Circuit Cross Reference Data (continued)

FOXBORO	Ţ. Ţ	NSC	SPRAGUE	MOTOROLA	FAIRCHILD	DEC	SIGNETICS
C3313AF	51174164						
C3313AG	SN7406-N						
C3313AH	SN7417						
C3313AJ	SW7437						
C3313AL							SP384A
C3313AP	SN74403		USN7440AJ	MC7440L			N7440F
C3313AQ	SN7474J		USN7474J				
C3313AR	SN740SJ		US7405J	MC7405L			
C3313AS	SN741213						N74121F
C3313AT			US7439H				
V3008EA	SN740GN	DMBODON	USN7400A	MC7400P			
V3008E8	SN7401N		USN7401A	MC7401P			
V3008EC	SN7402N		USH7402A	MC7402P			
V3008EE	SN7410N	0M8010N	USN7410A	MC7410P			
V3008EF	SN7420N	DM8020M	USN7420A				
V300BEK	SN7430M		USN7430A	RC7430P			
V3008EL	SN7440W	DM8040N	USN7440A	MC7440P	 -		

Table 1. Integrated Circuit Cross-Reference Oata (continued)

FOX80R0	T.I.	N.S.C	SPRAGUE	MOTOROLA	FAIRCHILO	0EC	SIGNETICS
V3008EN	SN7450N		USN74S0A	MC7450P			
V3008EP	SN7451N		US!(7451A	MC74S1P			
V3008ER	SN7453N		US7453A	MC7453P			
V3008ES	SW7454N		U57454A	MC7454P			
V3008ET	SN7460H		USW7460A	MC7460P			
V3008EW	SN7470N		US7470A				
V3008EX	SN7472N		SUN7472A	MC7472P			
V3008EY	5N7473N	0148501N	USN7473A	MC7473P			
V3008EZ	SN747411	OM8510N	U5N7474A				
V3008FA	5N7475N	0M8550W	U5N7475B	MC7475P			
V3008FB	SN7476N	01/85001	USN7476B	IAC7476P			
V3008FC	SN7480M		USN7480A				
V3008FE	SN7482N	,	U5N7482A				
V3008FF	SN7483N		U5N74838				
V3008FK	5N7490N	0K8530N	U5117490A				
V3008FL	SN7491AN		USN7491A				

Table 1. Integrated Circuit Cross-Reference Oata (continued)

FOXBORO	T.I.	N.S.C	SPRAGUE	MOTOROLA	FAIRCHILD	0EC	SIGNETICS
V3008FM	SN7492N	0M8532N	USN7492N				
V3008FN	SN7493N	OM8533N	USN7493A				
V3008FP	SN749411						
V3008FR	SN7495N						
V3008FS	SN7496N						

KEV.

FOX80RO = The Foxboro Company, Foxboro, Ma.

T. I. = Texas Instruments Inc., Oallas, Texas

N.S.C = National Semiconductor Corp., Santa Clara, Ca. FAIS

SPRAGUE = Sprague Electric Co., North Adams, Ma

MOTORLA = Motorola Semiconductor Products
Inc., Phoenix, Ar
FAIRCHILO = Fairchild Camera & Instrument
Corp., Mountain View, Ca
OEC = Oigital Equipment Corp., Maynard, Ma
SIGNETICS = Signetics Corp., Sunnyvale, Ca

CONTENTS

NAME	NUMBER	VERSION	SHEETS
Dual Line Oriver	C3002RR	Α	5
Hex Inverter	C3004NS	A	4
Quadruple 2-Input NANO Gate	C3004NT	А	5
Hex Inverter	C3004NW	В	4
Monostable Multivibrator	C3004PL	А	5
Hex Inverters	C3007/4R	8	6
Oual J-K Master-Slave Flip-Flops	C3008BZ	A	6
4 Line-to-10 Line Oecoder	C3008FL	Α	2
Oual J-K Flip-Flop	C3009SM	A	1
Buffer Storage Elements	0300988	Α	1
Nixie Decoder/Oriver	C3009ST	А	1
Quad 2-Input HOR	C3313AA	A	7
Quad 2-Input NANO	C3313AB	A	6
Hex Buffers/Orivers	C3313AC	В	6
Dual J-K Master-SLave Flip-Flops	C3313A0	A	6
Quadruple 2-Input Exclusive OR Gates	C3313AE	А	7
8-Bit Parallel-Out Serial Shift Registers	C3313AF	Α	5
Hex Inverter, Buffers/Orivers	C3313AG	A	7
Hex Buffers/Orivers	C3313AH	A	7
Quadruple 2-Input Positive NANO Buffers	C3313AJ	Α	3
Quad 2-Input Positive OR Gate	C3313AL	1A	5

CONTENTS (continued)

NAME	NUMBER	VERSION	SHEETS
Oual 4-Input Positive NANO Power Gate	C3313AP	А	4
Oual "O" Type Flip-Flop	C3313AQ	A	5
Six Inverters	C3313AR	Α	5
Monostable Multivibrator	C3313AS	Α	4
Quad 2-Input NANO Suffer	C3313AT	1A	3
Quadruple 2-Input Positive NANO Gate	V3008EA	А	5
Quadruple 2-Input NANO Gate	V300BEB	Α	7
Quadruple 2-Input NOR Gate	V300BEC	В	2
Triple 3-Input Positive NANO Gate	V3008EE	Α	5
Oual 4-Input Positive Gate	V3008EF	Α	5
Eight-Input Positive NANO Gate	V3008EK	Α	5
Oual 4-Input Positive NANO Power Gate	V3008EL	A	5
Oual 2-Wide 2-Input ANO/OR/Invert Gate	V300BEN/E	Р В	4
Quad. 2 ANO/OR/Invert Gate	V3008ER/E	s c	4
Oual 4-Input Expander	V3008ET	А	4
Single Phase J-K Flip-Flop	V3008EW	В	5
Single Master/Slave Flip-Flop	V3008EX	Α	5
Oual Master/Slave Flip-Flop	V3008EY	A	5
Oual "O" Type Flip-Flop	V300BEZ	A	6
Quadruple Latch	V3008FA	A	10
Oual Master/Slave Flip-Flop with Preset and Clear	V3008FB	A	4
Full Adder	V300BFC	Α	11
Two-8it 8inary Adder	V3008FE	Α	g
Four-8it 8inary Adder	V3008FF	A	10
Decade Counter	V3008FK	А	6
Eight-8it Shift Register	V3008FL	A	7

CONTENTS (continued)

NAME	RUMBER	VERSION	SHEETS
Divide By 12 Counter	V3008FM	Α	6
Four-Bit Binary Counter	V300BFN	A	6
Four-Bit Shift Register	V3008FP	Α	5
Four-8it Right/Left Shift Register	V300BFR	A	g
Five-8it Shift Register	V3008FS	А	6

		V .			
FIRST USED ON		REVISIONS			
C3001XX	LTR	DESCRIPTION	DR	DATE	APPROVED
	LA.	LOCAL RELEASE ECN 3035.	A.Z.	16DEC69	DEH

1. DESCRIPTION

FORM 5083A (6/67)

Circuit, Integrated (Dual In-Line Package) Dual Line Driver

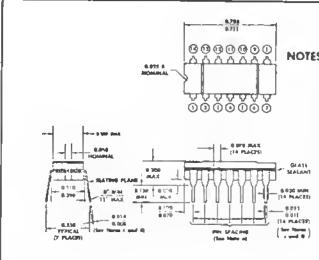
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 3,4,5
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN75110N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

NOTES:			DO NOT SCALE PRINT
UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.		FOXBORO THE FOXBORO COMPANY
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES	ORAFTSMAN A 7A.	OATE	FOXBURU, MASSACHUSETTS, U.S.A.
TOLERANCES ON	DESIGNER		TITLE: CIRCUIT, INTEGRATED
RACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	CHECKER	1400069	DUAL TREATME DAGGER
MATERIAL:	ENGINEER		SIZE SYMBOL DRAWING NO. REV
FINISH:	RELEASED		A B [C3002RR A
L	LOCAL KELEASE		SCALE: NONE SHEET LOF 5





NOTES: a. The true-position pin spacing is 0.100 between conterlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins. (4)

of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

 This dimension does not apply for solder-dipped leads.

4

d. Witen solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0,020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

NOT SCALE PRINT

4 50838 (6/67)

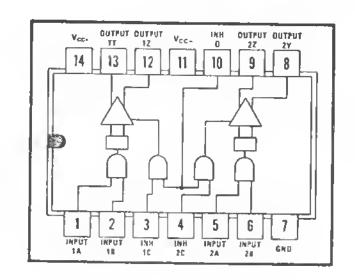
TYPES SN55109, SN55110, SN75109, SN75110 DUAL LINE DRIVERS

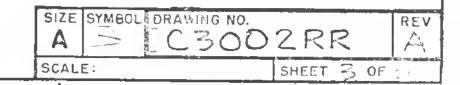
logic

TRUTH TABLE

LOGIC	INPUTS	INHIS	SITOR UTS	ουτι	PUTS
Α	8	C	D	Y	Z
LorH	L or H	L	LorH	Н	Н
L or H	LorH	LorH	Ļ	Н	Н
L	LorH	Н	Н	Ļ	Н
LorH	Ļ	Н	Н	L	Н
Н	Н	Н	Н	Н	L

Low output represents the on state High output represents the off state





absolute maximum ratings (over operating free-air temperatura range unlass otherwise noted)

Supply voltage V _{CC+} (See Note 1)	7 V
Supply voltage V _{CC} . (See Note 1)	_7 V
Logic and inhibitor input voltages (See Note 1)	55 V
Common-mode output voltage (See Note 1)	12 V
Operating free-air temperature range, Series 55	25°C
Series 75	70°C
Storage temperature range, ceramic dual-in-line (J) package	50°C
plastic dual-in-line (N) package	50°C

recommended operating conditions (see note 2)

		SN65104 SN5511		\$	UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage VCC+ (See Note 1)	4.5	5	5.5	4.75	5	5.20	V
Supply voltage V _{CC} _(See Note 1)	-4.6	-5	-5.5	-4.75	-6	-5.25	V
Positive common-mode output voltage (See Note 1)	0		10	0		16	٧
Nenative common-mode output voltano (See Note 1):	D		-3	0		-3	V
Operating free-air temperature rango	<i>-</i> 85 125		0		70	°C	

NOTES: 1. These voltage values are with respect to the network ground terminal.

2. When using only one chennel of the fine drivers, the other chennel should be inhibited end/or its outputs grounded.

568

SIZE SYMBOL ORAWING NO.

A C C 3002RR A

SCALE: SHEET 4 OF 5

O NOT SCALE PRINT

MM 5083B (6/67)

electrical characteristics (over operating free-air temperature range unless otherwise noted)

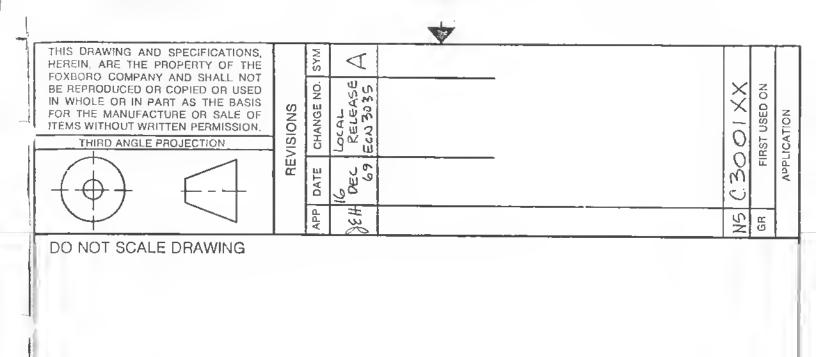
	PARAMETER	TEST	TEST CO	NOITIONS!				SN55110, \$1475110				
		FIGURE			MIN	TAb:	MAX	MIN	TYPS	MAX	UN	
Томпър	High-level input	16	V _{CC+} = MAX, V _{IHILI} = 2.4 V	V _{CC} MAX.			40			40	p)	
	1A, 1B, 2A or 28		V _{CC+} = MAX, V _{THRLI} - MAX V _{CC}	V _{CC} - + MAX,			1			1	m	
lin(n)	Low-level input current into 1.A, 18, 2A or 28	15	V _{CC+} - MAX, V _{ILELI} + 0.4 V	V _{CC-} * MAX,			-3			-3	m	
(1HHI)	High-level input	17	V _{CC+} = NAX, V _{[St[])} = 2.4 V	V _{CC} MAX,			40			40	μ/	
	1C or 2C		V _{CC+} = MAX, V _{IHII)} = MAX V _{CC+}	V _{CC} MAX,			1			1	m	
וויוון	Low-level input current into TC or 20	17	V _{CC+} = MAX, V _{ILIII} = 0.4 V	V _{CC} - * MAX,			-3			-3	m	
 	High-level input	17	V _{CC+} * MAX, V _{IHIII} + 2.4 V	V _{CC-} - MAX,			BQ			80	μ,	
-1801	current into D	, ,	VCC+ - MAX, VIHIII - MAX VCC+	V _{CC} - + MAX,			2			2	m	
lirii)	Low-level input current into D	17	V _{CC+} + MAX, V _{ILID} + 0.4 V	V _{CC} MAX,			-6			-6	m	
Oloni	On-state output current	18	V _{CC+} + MAX, V _{CC+} + MIN,	Vcc- = MAX Vcc- = MAX	3.5		7	6.5		15	m.	
1010111	Off state output current	18	VCQ+ * MIN.	V _{CC} M/N			100			100	μ/	
CC+lon1	Supply current from VCC+ with driver enabled	19	VILILI *0 4 V.	V _{[H[I]} = 2 V		18	30	-	23	35	m.	
CC-tonl	Supply current from VCC_ with driver mebled	19	VILIL) - 0.4 V.	V _{DHH} - 2 V		-18	- 30	_	-34	-50	_	
CC+[ef]]	Supply current from VCC+ with driver inhibited	19	VILILI - 04 V.	V _{IL(II)} =0.4 V		18		_	31		m	
CC-(o) f)	Supply cuttent from VCC+ with driver inhibited	19	VILILI = 0.4 V.	V _{IL[I]} = 0.4 V		~10			-17	\neg	m	

[‡]For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable

device type. § All typical values are at $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $Y_A = 25 \text{ C}$. switching characteristics, VCC+=5 V, VCC-=5 V, $Y_A = 25 \text{ C}$

	PARAMETER		TEST CO	VOLLIONS	МІМ	TYP	MAX	UNIT
IPLHILI	Propagation dalay (ime, low-to-high level, from logic input A or 8 to outbut Y or Z	20	RL = 50 st.	CL = 40 pF		9	15	nı
(PHLIL)	Propagation datay time, high-to-low-level, from logic Input A or 8 to autput Y or Z	20	R _L = 50 Ω,	CL - 40 pf		9	15	m
PLHIII	Propagation delay time, low-to-high- level, Itom inhibitor input C or D to output Y or Z	- 20	R _L = 50 H,	CL - 40 pF		16	25	na
PHL(†)	Propagation dalay time, high-to-low level, from inhibitor input C or D to output Y or 2	20	R _L - 50 Ω,	CL - 40 pF		13	25	ris

SIZE SYMBOL DRAWING NO. REV C3002RR SCALE: SHEET



1. DESCRIPTION

Circuit, Integrated (dual in-line package) hex inverter

2. PHYSICAL CHARACTERISTICS

See Sheet 2

3. PERFORMANCE CHARACTERISTICS

See Sheet 3 & 4

4. MANUFACTURER'S NAME & PART NO.

Texas Instruments, Part No. SN75107N

	PRINT	DISTR
- 1	DEPT	OTY
		-
i		
		-

FOR PARTS LIST SEE DWG PL

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED SH	DATE 160ECLA	FOX	50RO	_	BORO COMPANY SSACHUSETTS, U	.S.A.		
.X .XX .XXX ± ±.04 ±.010 ANGLES ± FRACTIONS = .028 DIA MATL	DRAFTING	Circuit Integrated							
FINISH	RESTRICTED RELEASE LOCAL RELEASE CORPORATE RELEASE	160E4g	SIZE DWG CODE	WI	DRAWING NU	MBER 04NS SHEET OF	A REV		

- . 6711 6711 TYPRES TAAAAA

NOTES: a. The true-position pin specing is 0.100 between tweetodinos. Each per centeralis located within 200.010 of its to a longitudinal partition relative to plus (4)

b. All diminations in inchas unless otherwise caused.

c. This dimension does not apply for solder-disped

lowers.

4

d. A non-solder-diamed leads are meetined if aged area of the had a securitem the lead tip to arise it 0.020 in the currently stating plans.

e. Ali JEDCC TO-116 notes apply.

14-PIN FUNCTIONS

SIZE SYN BOES CRAVILLE NO. C3004NS SCALE: SHEET 2 GF

HOT SCALE PRINT

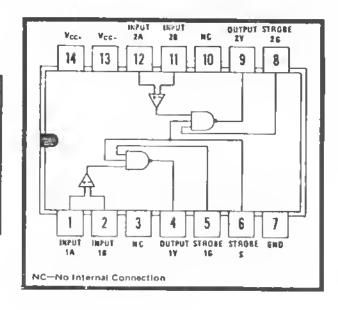
30838 (6/67)

TYPES SR55107, SR55103, SN75107, SN75108 DUAL LINE RECEIVERS

logic

TRUTH TABLE

DIFFERENTIAL INPUTS	STR	DBES	ОПТРИТ
A-B	G	S	Υ
V _{ID} ≥ 25 mV	LorH	L or H	н
	L or H	L	н
-25 mV < V _{ID} < 25 mV	L	L or H	H
	Н	H	INDETERMINATE
	L or H	L	н
V _{ID} ≤~25 mV	L	L or H	Н
	Н	н	L



SIZE SYMBOLE DRAWING NO.

A S C 3004NS A

SCALE: SHEET 3 OF 4

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4 5083B (6/67)

absoluta maximum ratings (over operating free-air temperatura range unless otherwise noted)

Const. In the second of the se	
Supply voltage V _{CC} . (See Note I)	7 V
Supply voltage V _{CC} . (See Note 1)	7 V
Differential input voltage (See Note 2)	±6 V
Common-mode input voltage (See Note 1)	±5 V
Stilobe input voltage [See Note 1]	5.5 V
Operating free-air temperature range, Series 55	to 125°C
Series 75	C to 70°C
Storage temperature range, ceramic dual-in-line (J) package	to 150°C
plastic dual-in-line (NF package	to 150°C

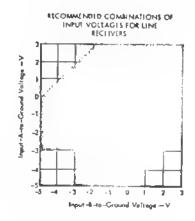
recommended operating conditions (see note 3)

	SN5	5107, SN	155103	SN75			
	MIN	Nota	MAX	MUN	NOM	ALAX:	UNIT
Supply voltage: V _{CC1} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage: V _{CC} , (See Note 1)	-4.5	-5	-55	-4.75	-5	-5.29	
Objput sink current			-16			-16	mA
Differential input voltage (See Notes 2 and 4)	-51		5	-51		5	V
Common-mode input voltage (See Notes 1 and 4)	-31		3	-31		3	V
Input voitage tange, any differential input to ground ISee Note 41	- 51		3	-51			-
Queleting flee-eir temperature tenge	-55		125	0		70	-62

NOTES: 1. These voltage values are with respect to network ground terminet.

- These voltage values are at the noninverting (+) terminal with respect to the inverting (-) terminal.
- When using only one chennel of the line receiver, the inputs of the other channel should be grounded.
- The recommended combinations of input voltages fell within the shaded area of the figure at the right.

The eigebraic convention, where the most positive limit is designated maximum, is used in this data sheet with logic input voltage levels only.



SIZE SYMBOL DRAWING NO.

A C 3004NS A

SCALE: SHEET 4 OF 4

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5083B (6/67)

		REVISIONS			
L	LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
	A	LOCAL RELEASE PER ECH 3035		16 DEC 69	J.E.H.

1																		
	REV STATUS	REV	A	А	A	A	A											
	OF SHEETS	SHEET	1	2	3	4	5	6	7	В	9	10	11	12	13	14	15	16
	TOLERANCES UNLESS OTHERWISE S DECIMAL DIMENSION ANGLES	PECIFIEO	DRAWN J.F. 1 DRAFTING	4- 1-	K'D E. +/,	· 0	ATE	FO)XI	30F	20						PANY TS, U	. S. A.
			DESIGNEO							D	VAI	ر ا ا ا	J-L	INE	PAG	2KA		0
I	SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES ND	LOCAL RELEASE		, 41,	10	ár r	SIZE		P	>			ORAW 30				-
Į	DESIGNED FOR		CORPORAT RELEASE					SCALE				W	'n	SH	EET	1 (OF 🖫	,
	ORM 5758LT (5/60)		·					A										

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package) Quadruple 2-input NAND gate with open collector output.

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 3.
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheets 4 & 5.
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7403N

Sprague Part No. USN7403 National Semiconductor Corp. DM8003N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

A B C3004NT A

SCALE: SHEET 4 OF

d grij 1 de(las m.s.		**************************************	Note
# 1 100 MA # 100 M # 100 M	manufut m	O 079 of 1 Phás I Thuật I Phás	- Gottl - Mileset - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1

5: a. The tive-notition pin strating is 0.100 between cantailines, buth pur contailine is located within #0.010 or its this tanginodinal position relative to pilit (4) as the first

b. All distinuishers in inches unless otherwise noted,

c. This dimension does not apply for solder-dipped teu.h.

d. Wann raldand, need leads are specified dipped area of the leading of the in the leading to at least 0.020. into alsows the secting plane.

e. All JOSC 70-116 notes apply.

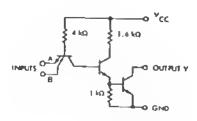
14-PIN FUNCTIONS

SIZE SYN'BOLF CONTING NO. $e^{\alpha i \frac{1}{2}}$ SCALE: SHEET

HOT SCALE PRINT

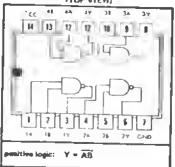
130838 (6/67)

schematic (each gate)



NOTE: Component values shown are nominal.

JOR N DUAL-IN-LINE PACKAGE ITOP VIEW)



SIZE SYMBOLDRALHIG NO.

A B CBOOGANT

SCALE: SHEET 4- OF

O NOT SCALE PRINT

× 50519 (6/47)

recommended operating	conditions							MIN	NOM	414.9	UNIT
								MILL	SACISM	MAA	UNIT
Supply Voltage VCC:	SN5403 Circuits							4.5	5	5.5	V
	SN7403 Circuits							4.75	5	5.25	V
Normalized Fan-Out F	rom Each Output, N (4	nd see pa	ges 2-7	and 2-8	3).					10	
Occasion Eron Air Tor	maratura Dance Tax	CNEAD	2 Circu	ite					0.5	400	0

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

SN7403 Circuits

	PARAMETER	TEST FIGURE	TEST CONDITIONS!	MIN TYP:	MAX	UNIT
V _{in(1)}	Logical 1 input voltage required el both input ferminals to ensura logical 0 (on) level et output)	1	V _{CC} - MIN	2		v
Vin(0)	Logical 0 input voltage required et either input terminal to ensure logical 1 (off) level et output	7	VCC - MIN. VIN- 0.8 V		8.0	٧
loui(1)	Output reverse current	7	V _{CC} • MIN. V _{IN} • 2 V. V _{OUI(1)} • 5 5 V		250	μА
V _{pul} (0)	Lögicet 0 övi put voltaga (on levet)	t	V _{CC} = MIN, I _{SINk} = 16 mA		0.4	٧
0)لاتا	Logical 0 level input current (each input)	з	V _{CC} - MAX, V _{in} - 0.4 V		1.8	mA
lin(1)	Logical 1 level input current (each input)	4	V _{CC} • MAX. V _{In} = 24 V V _{CC} • MAX, V _{In} = 5.5 V		40	μA mA
Iccioi	Logical D level supply current	6	V _{CC} = MAX, V _{in} = 5 V	12	22	mA
¹ CC(1)	Logical 1 level supply current	6	V _{CC} = MAX, V _{in} = 0	4	8	mA

switching characteristics, VCC = 5 V, TA = 25°C

	PARAMETER		TEST C	MIN	TYP	MAX	UNIT	
IpdQ	Propagation delay time to logical 0 level	65	CL • 15 pF.	Я _L = 400 ก		8	15	P1
4pdt	Programion dalay time to logical 1 level	65	C _L = 15 pF,	អ _L • 4 ៤ន		35	45	nı

Equipment of the second second

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SIZE SYMBOL DRAWING NO.

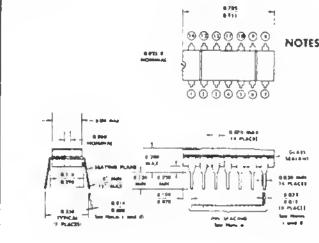
A B C 3004 NT A

SCALE: SHEET 5 OF 5

¹ All typical values are at V_{CC} = 5 V⁺T_A = 25°C.

	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 3035		DECGO	JOHN HATCH
B	REVISED & REDRAWN PER ECN 4398		22 JAN 73	w. J.J.

			CON	PORATE				475	SCALE				Tw			IEET		OF /p	
SUPERSEDING INTERCHANGEABLE SIMILAR TO		es Es	LOCA RELE	AL					A		B			L		O4NN		ER	
			E	GNED						Pur tegra	chas ated	e St Cir Type	ec. cuit	7404	И				
TOLERANC UNLESS OTHERWISE DECIMAL DIMENSION ANGLES	SPE INS :	_	DRAI	E. F	1 7.	Ē.H	DE C	TE _ 72_))([:	OR		FOXB	ORO,		ORO (SACH			s A
OF SHEET	3	SHE	EET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
REV STATU	IS	RE	V	\mathcal{B}	B	B	P												
SHEET 17	1	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
REV	1																		
SHEET 3	5	37	38	39	40	41	42	43	44	45	46	47	48	49	50				
REV	\top																		
SHEET																			
REV					1			L	1		1								



- NOTES: a. The true-position pin specing is 0,100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) ond 🕕
 - b. All dimensions in inches unless otherwise noted.
 - c. This dimension does not apply for solder-dipped leads.
 - d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch obove the seating plane.
 - e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

#19.1

SIZE SYMBOL DRAWING NO. REV)04NW SCALE: SHEET 🙎

NOT SCALE PRINT

1.0 <u>DESCRIPTION</u>

Circuit, Integrated (Dual In-Line Pkg. hex inverter)

- 2.0 REQUIREMENTS
- 2.1 Electrical: See Table 1 (Sheet 4)
- 2.2 Mechanical: See Figure 1 (Sheet 2)
 - 3.0 VENDOR

Texas Instrument Part No. SN7404N

Sprague Part No. USN7404

Motorola Part No. MC7404P

National Semiconductor Corp. Part No. DM8004N

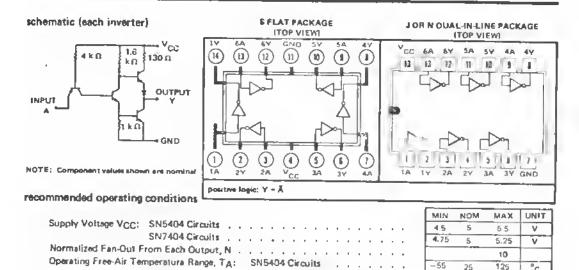
SIZE SYMBOL DRAWING ND.

A B C3004NW

SCALE: SHEET 3 OF 4

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TABLE



SN7404 Circuits electrical characteristics (over recommended operating free-eir temperature range unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CO	OITION	NS [‡]	MIN	TAbt	мах	וואט
Vin(1)	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	16	V _{CC} • MIN			2		_	v
V _{In(0)}	Logical 0 input voltage required et any input terminal to ensure fogical 1 level at output	16	V _{CC} = MIN					0.8	v
Vout(1)	Logical 1 output voltage	15	V _{CC} = MIN, I _{load} = -400 μA	V _{in} •	0.8 V.	2,4	3.3		v
Vouttoi	Logical 0 output voltage	15	V _{CC} = MIN, I _{sink} = 16 mA	V _{In} -	2 V.		0.22	0.4	V
Jin(0)	Logical D level input current (each Logical D level input current	17	Vcc - MAX.	Vin -	0,4 V		_	-1.6	mA
lin(1)	Logical 1 level input current	18	VCC = MAX,	Vin = :	2 4 V			40	μА
111(17			VCC = MAX,	V _{in} = 3	5.5 V			1	mA
los	Short-circult output current!	19	V _{CC} - MAX		SN5404	-20		-55	
	Grotteneoit output commits	. "		[SN7404	18		-55	mA
lecioi	Logical 0 level supply current	20	V _{CC} • MAX,	V _m = !	5 V		18	33	mA
^l echt	Lógical 1 level supply current	20	VCC - MAX.	V _{In} = ()		6	12	mA

switching characteristics, VCC = 5 V, TA = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST (CONDITIONS	MIN	TYP	MAX	UNIT
^L pdQ	Propagation delay time to logical Q level	65	C _L = 15 pF,	RL = 400 ß		8	15	ns
\pd1	Propagation delay time to logical 1 level	65	CL • 15 pF,	RL = 400 Ω		12	22	ns.

t For conditions shown as MtN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type,

SIZE SYMBOL DRAWING NO. REV 3004NW B SCALE: SHEET 4 OF 4

NOT SCALE PRINT

50838 (6/67)

All typical values are et V_{GG} = 5 V, T_A = 25°C.

I Not more than one output should be shorted at a time.

	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
	ISSUED ECN NO. 3070		15 JAN 70	

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	REV STATUS	REV	A	A	A	Δ_c	Д											
	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	.12	13	14	15	16
	TOLERANCES UNLESS OTHERWISE SPECIFIED DECIMAL DIMENSIONS ± .02D ANGLES DESIGNED DRAWN A ZILAS DRAWN A ZILAS DRAWN A ZILAS DRAWN A ZILAS DRAFTING THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.																	
			DESIGNED				CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN 74121											
ı	SUPERSEDING INTERCHANGEABLE SIMILAR TD	YES ND	LOCAL RELEASE		(TCH	15,4	SIZE DRAWING NUMBER C3004PL											
	DESIGNED FOR		CORPORAT RELEASE E	E. FR	ANKLI	N 5,	- بمريو	SCALE				w	т	SH	EET	1 0	DF 5	-
-	DRM 5758-C (5749)							A										

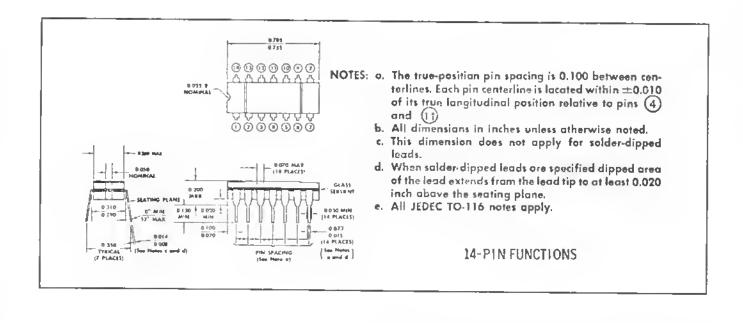
いな様には特殊は無対けれて利を発表がはは時には必要に

1. DESCRIPTION

Circuit, Integrated (Dual in-line package) mono stable multivibrator.

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 3.
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 4.
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instruments Part No. SN74121



THE FOXBORO COMPANY SYSTEMS DIVISION

BJ

C3004 PL

Rev.

Sheat 3 of

CIRCUIT TYPES SNS4121, SN74121 MONOSTABLE MULTIVIDRATORS

logic

TRUTH TABLE (See Notes 1 thru 3)

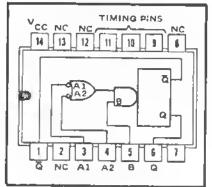
\$ _n	INPL	IT .	t _{n+1}	INPL	JΤ	OUTPUT
A1	A2	В	A1	AZ	В	COTPOT
\Box		0			1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	Х	One Shot	
X	0	0	X	0	1	One Shot
1	1	1	x	0	1	One Shot
1	1	1	0	x	1	One Shot
X	0	0	х	1	0	Inhibit
0	X	0	1 1	х	0	Inhibit
X	0	1 :	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	х	0	0	Inhibit
1	1	0	0 X 0			Inhibit

1-V_{in(1)}>2V 0-V_{in(0)}<0.8 V

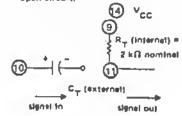
NOTES: 1. t_n = time before input transition,

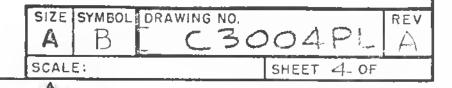
- 2. t_{n + t} = time efter input trensition.
- X indicates that either a logical 0 or 1, may be present.
- 4. NC = No Internel Connection.

J OR N OUAL-IN-LINE PACKAGE (TOP VIEW) (SEE NOTES 6 THRU 9)



- A1 and A2 are negative-edge-triggeredlogic inputs, and will trigger the one shot when either or both go to logical 0 with β at logical 1.
- 6. B is a positive Schmitt-trigger input for allow adges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
- 7. Externel timing capacitor may be connected between pin (1) (positival and pin (1). With no externel capacitance, an output pulse width of typically 30 nails obtained.
- To use the internel timing resistor (2 kΩ nominel), connect pin 9 to pin 64.
- 9. To obtain veriable pulse width connect external veriable resistance between pin and pin No external current limiting to needed.
- 10. For eccurete repeatable pulse widths connect an external resistor between pin 10 and pin 14 with pin 19 open-circuit.





CIRCUIT TYPES SNS4121, SN74121 MONOSTABLE MULTIVIBRATORS

electrical characteristics over operating free-air temperature range

	PARAMETER	TEST FIGURE	TEST CONDITIONS		MtN	TYP‡	MAX	ידואט
V _{T+} Posi	tive-going threshold voltage at A input	6.7	V _{CC} - MIN			1.4	2	V
	trive-poing threshold volue MinI A input	57	V _{CC} - MIN		0.8	1,4		V
	overgroup threshold so tank at 6 input	57	Y _{CC} - MIN			1.55	2	V
V _T _hegs	tive-going thieshold voltage at B input	57	V _{CC} = MIN		8.0	1.35		٧
Vout(0)	Logical D output vottege	57	VCC = MIN, Isink = 16 mA			0.22	0.4	V
Vout(1)	Logical 1 output voltage	67	VCC = MIN, I load = -400 µA		2.4	3.3		v
in(0)	Logical D level input current at A1 or A2	58	V _{CC} = MAX, V _{in} = 0.4 V			-1	-1.6	mA
in(O)	Logical D level input current at B	59	VCC - MAX, Vin - 0,4 V			-2	-3,2	mA
In(1)	Logical 1 level input	60	V _{CC} = MAX, V _{SC} = 2.4 V		-	2	40	μΑ
· IIH(I)	current at A1 or A2		V _{CC} = MAX, V _{in} = 5.5 V			0.05	1	mA
in(1)	Logical 1 level input	61	VCC = MAX, Vin = 2.4 V			4	80	μΑ
107(1)	current et B		VCC - MAX, Vin - 5.5 V			0.05	1	mA
	Short circuit output	62		SN54121	-20	-25	-55	
os .	current at Q or Q1	end 63	V _{CC} = MAX	SN74121	-18	-25	-55	mA
lcc	Power supply current in quiescent (unfired) state	64	V _{CC} = MAX			13	25	mA
cc	Power supply current in fired state	64	V _{CC} = MAX			23	40	mA

tför conditions shown as MIN or MAX, uss the appropriate value specified under recommended operating conditions för the applicable

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST FIGURE	TEST	MtN	TYP	MAX	UNITS	
t _{pd1}	Propagation dalay time to logical 1 level from 8 input to 0 output	72		0 - 00-5	t5	35	55	ni
t _{pd1}	Propagation datay time to logical 1 leval from A t/A 2 inputs to Q output	72	CL • 15 pF,	C _T = 80 pF	25	45	70	ns.
t _{pd0}	Propagation dailby time to logical Office I from 8 import to Q output	72			20	40	65	PM
^t pd0	Propagation daily time to logical O level from A1/A2 inputs to 0 output	f 4	C _L = 16 pF,	C _T = 80 pF	30	50	80	ПE
^t p(out)	Pulse width obtained using internal liming resistor	73	C _L = 15 pF, R _T = Open,	CT = 80 pF, Pin ③ to V _{CC}	70	110	150	mi
tp(out)	Pulse width obtained with zero timing capacitance	73	Ct = 15 pF, RT = Open,	CT = 0, Pin ③ to V _{CC}	20	30	50	nı
(plout)	Pulse width obtained using	73	CL = t5 pF. RT = t0 kft,	Ст = 100 pF, Ріп (₃ Ореп	600	700	800	1.11L
Piouti	external timing resistor	1.0	CL = 19 pF. RT = 10 kΩ,	Cy = 1 aF. Pin (1) Open	6	7	8	ens
Phold	Minimum duration of trigger pulse	73	C _L = 15 pF, R _T = Open,	CT = PO pF, Pm ① to V _{CC}		30	50	THE

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SIZE SYMBOL DRAWING NO. REV C3004PL Α SCALE: SHEET 5 OF 15

^{\$}All typical values are at V_{CC} = 5 V, T_A = 25°C, § Not more than one output should be shorted at a time,

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	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
B	ECH NO. 3919		3/0071	W.T.

13 90 17																			
1	REV STATUS	REV	B	B	Po	B	E	B											
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		OESIGNEO					CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN74051J												
ı	SUPERSEDING INTERCHANGEABLE SIMILAR TO	LOCAL RELEASE. POLINIAN			. 22	er e	SIZE		B			DRAWING NUMBER C3007MR							
2	DESIGNEO FOR	CORPORATE RELEASE S. F.O. GANKLIKA			1 1	133	SCALE				W	WT SHEET 1 OF G							

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package) Hex Inverters (with open collector output)

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 3.
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 5.
- 4. MANUFACTURER'S NAME AND PART NO.

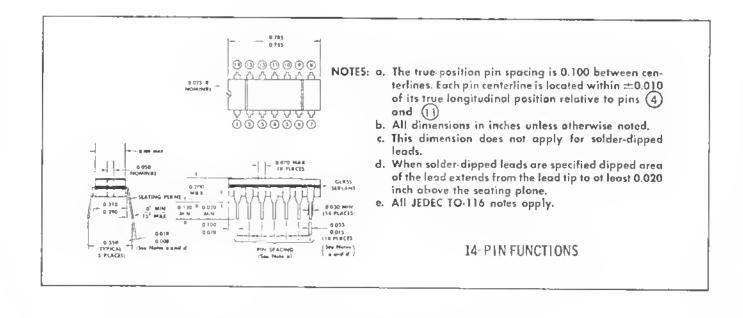
Texas Instrument, Part No. SN7405N Sprague Part No. USN7405A Motorola Part No. MC7405P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

A E C3007MR B

SCALE: SHEET 2 OF



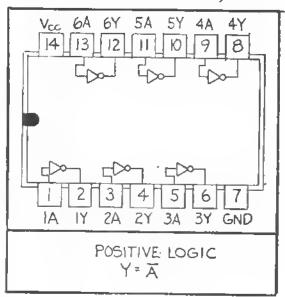
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Sheet

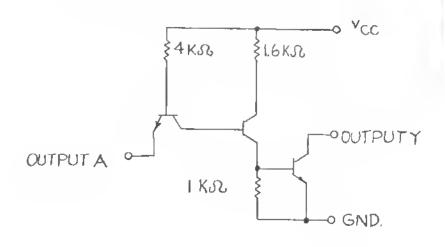
THE FOXBORO COMPANY

SYSTEMS DIVISION

JORN DUAL-IN- LINE PACKAGE (TOP VIEW)



SCHEMATIC (EACH GATE)



SIZE SYMBOL DRAWING NO.

A B C3007 MR

SCALE: 40

SHEET -1 OF

DO NOT SCALE PRINT

FORM 50838 (6/67)

RECOMMENDED OPERATING CONDITIONS SUPPLY VOLTAGE - 4.75-5.25V

CHARACTERISTICS (OVER BECOMMENDE ELECTRICAL

TURE

<u> </u>	INICAL CHARACIERISILOS LOVER RECOMMENDED OPERATING FREE-AIR TEMPERAT	77.X T	ECOMMENDE	D OPERATING	, FREE-AIR TEN	1PERA
	PARAMETER	TEST	TEST CON	TEST CONDITIONS +	MIN TYP * MAX	FIND
	LOGICAL I INPUT VOLTAGE IN(I) TO ENSURE LOGICAL I (OFF) LEVEL AT OUTPUT	15.	CC = M.		ما	>
	LOGICAL O INPUT VOLTAGE REQ'D, AT INPUT TERMINAL TO ENSURE LOGICAL I (OFF) LEVEL AT OUTPUT,	9	CC = MIN.		80	>
	OUT(1) OUTPUTREVERSE CURRENT	5	"CC = MIN, "OUT(1) = 55V	VBO-NI	250	μA
	SUT(0) LOGICAL O OUTPUT VOLTAGE (ON LEVEL)	75	CC = MIN	>2 = ZI	4.0	>
	TIN(O) LOGICALO LEVEL INPUT CURRENT	17	VCC = MAX ,	VIN=0.4V	9:-	₹ %
	TIN(I) LOGICAL I LEVEL INPUT	<u>«</u>	CC = MAX,	V _{IN} - 2,4 V	04	W.A
	CURRENT)	VCC = MAX,	VIN = 5.5 V		2nd
	CC(0) LOGICAL O LEVEL SUPPLY CURRENT	20	VCC * 5V TA : 25°C	>5 = NT _{>}	18 33	A MC
	CC(1) LOGICAL 1 LEVEL SUPPLY CURRENT	02	VCC = 5V TA = 25°C	0 "ZH>	6 12	JW.A
1						_

JOTES:

I. + FOR CONDITIONS SHOWN AS MIN OR MAX, USE THE APPROPRIATE VALUE SPECIFIED UNDER RECOMMENDED OPERATING CONDITIONS FOR THE APPLICABLE DEVICE TYPE,

THESE TYPICAL VALUES ARE AT VCC = 5V, TA = 25°C.

SIZE SYMBOL DRAWING NO.

A B C C 3007 MR B

SCALE: 76 SHEET 5 OF

DO NOT SCALE PRINT

FORM 50838 (6/67)

SWITCHING CHARACTERISTICS, "CC = 5V, TA = 25°C

L	DARAMETER	TEST		CALL CONT. LABOR	1
		FIGURE	LEGIT COINCITIONS	TAD XXX LAT L'AGAI	
May	PROPAGATION DELAY TIME TO LOGICAL Ø LEVEL	65	65 CL= 15PF, RL= 400 2	8 0	o Z
PDI	PROPAGATION DELAY TIME TO LOGICAL I LEVEL.	65	CL= 15 PF, RL= 4 D	40 55	v Z

SIZE SYMBOL DRAWING NO.

A B C 3007 MR B

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FORM 5083B (6/67)

L		REVISIONS			
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1	A	LOCAL RELEASE PER ECN. 3146		MAR 70	J.E.H.

FIRST USED ON: C 3001XX

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OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
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		DESIGNED			\top							TITLE					
					+				ircu ual					Тур	e SI	N741	07
SUPERSEDING INTERCHANGEABLE	YES	APPROVE	D				SIZE			Т	DRAWING NUMBER						
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DESIGNED FOR		CORPORA RELEASE		الكلالا	27 1 A <u>c</u>	673	SCALE					T	SH	EET	1 (OF 6	,
					_		A										

1.0 DESCRIPTION:

Circuit, Integrated (Dual In-Line Package)
Dual J-K Master-Slave Flip-Flops

- 2.0 PHYSICAL CHARACTERISTICS:
 - 2.1 See Sheet 3.
- 3.0 PERFORMANCE CHARACTERISTICS:
 - 3.1 See Sheet 5.
- 4.0 MANUFACTURER'S NAME AND PART NO.:

Texas Instrument, Part No. SN74107

Note: Only the item descibed on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

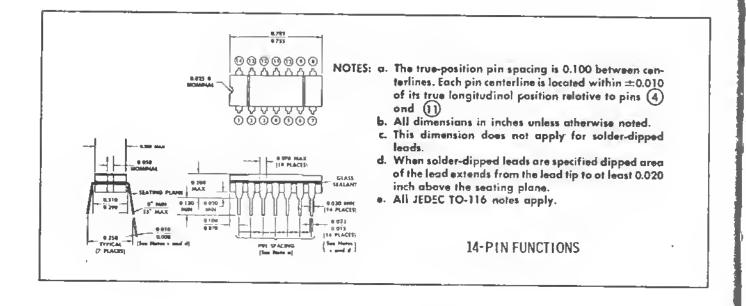
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FORM 4818-088-4/88

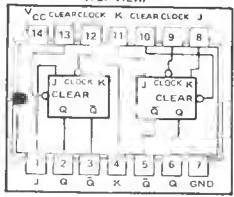


THE FOXBORO COMPANY SYSTEMS DIVISION

B < 3008 BZ

Sheet 3 of 6

SN74107 J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input to clear sets Q to logical O. Clear is independent of clock,

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: (See waveform on page 2-26)

- 1. Isolate slave from master
- 2. Enter information from J and K inputs to master
- 3. Disable J and K inputs
- 4. Transfer information from master to slave.

logic

	UTH T	
1	n	t _{n+1}
J	K	a
0	0	Qn
0	î	0
t	0	t
1	1	ā _n

MAX UNIT

NOTES: 1, t_n = 8lt time before clock pulse. 2. In+1 = Bit time efter clock pulse.

NOM

recommended operating conditions

Supply Voltage V_{CC}: SN5473, SN54107 Circuits SN7473, SN74107 Circuits Operating Free-Air Temperature Range, TA: SN74107 Circuits Normalized Fan-Out From Each Output, N Width of Clock Pulse, targetter (See Figure 69)

		(11177)	WITT
4,5	5	5.5	V
4.75	5	5.25	V
55	25	125	°C
0	25	70	°c
		10	
20			ns.
25			ns.
≥tp(clock)			
0			

SHEET 4 OF

6

4,5	5	5.5	V
4.75	5	5.25	V
55	25	125	°C
0	25	70	"C
		10	
20			ns
25			ns
≥tp(clock)			
0			

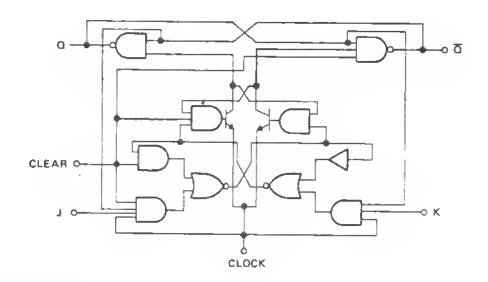
p(clock) (See Figure 69).			-		
Width of Clear Pulse, tp(clear) (See Figure 70) .	-				
Input Setup Time, t _{setup} (See Figure 69)					
Input Hold Time, thold					

SIZE SYMBOL DRAWING NO. REV < 3008 BZ A SCALE:

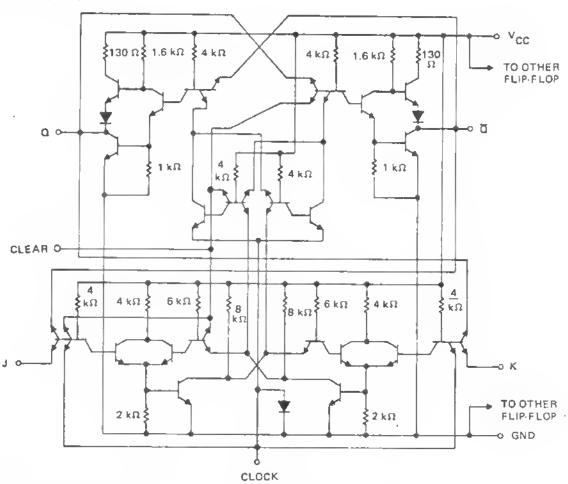
MIN

DO NOT SCALE PRINT

functional block diagram (each flip-flop)



schematic (each flip flop)



NOTE: Component values shown ere nominal,

SIZE SYMBOL DRAWING NO.

A B C3008BZ A

SCALE: SHEET 5 OF 6

FORM 50838 (6/67)

DO NOT SCALE PRINT

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST FIGURE		TEST CONOIT	IONS [†]	MIN	TYP‡	MAX	UNIT
	Input voltage required to	46							
Vin(1)	ensura logical 1 at any	and	VCC = MIN			2			V
	input terminal	47				Į			
	Input voltage required to	48			_				
Vin(0)	ansura logical 0 at any	and	VCC = MIN					8.0	V
	input terminal	47							
Vout(1)	Logical 1 output voltage	46	V _{CC} = MIN,	l _{load} = -4	00 μΑ	2.4	3,5		V
Vout(0)	Logical 0 output voltage	47	V _{CC} = MIN.	I _{sink} = 16	mA		0 22	0.4	V
l _{in} (0)	Logical 0 level input current at J or K	48	VCC = MAX,	V _{in} = 0.4 \	/			-1.6	mA
lin(0)	Logical O level input current at clear or clock	48	V _{CC} = MAX,	V _{in} = 0.4 \	/			-3.2	mA
1	Logical 1 level input current	40	V _{CC} = MAX,	V _{in} = 2.4 \	,	$\overline{}$		40	uА
lin(1)	at J or K	49	VCC = MAX,	V _{in} = 5.5 \	/			1	mA
4 4-1	Logical 1 level input current	- 10	VCC = MAX,	V _{in} = 2.4 \	/			80	μА
¹ in(1)	at clear or clock	49	VCC = MAX,	V _{in} = 5.5 \	/			1	mA
	51		V _{CC} * MAX		SN5473, SN54107	-20		-57	
los	Short-circuit output current§	50	- + CC (817/2	. vin - 0	SN7473, SN74107	- 18		-57	mA
lcc	Supply current	49	VCC = MAX,	V _{in} = 5 V			20	40	mA

[‡] For conditions shown as MIN or MAX, use the appropriets value specified under recommended operating conditions for the applicable

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, N = 10

	PARAMETER	TEST FIGURE		TEST CONDITIONS	MIN	TYP	MAX	UNIT
fclock	Maximum clock frequency	69	Cլ = 15 pF,	R _L = 400 Ω	15	20		MHz
tpd1	Propagation delay time to logical 1 level from clear to output	70	CL = 15 pF,	RL = 400 Ω		16	25	ns
t _{pd0}	Propagation delay time to logical 0 level from clear to output	70	CL = 15 pF,	R _L = 400 Ω		25	40	ns
^t pd1	Propagation delay time to logical 1 level from clock to output	69	C _L = 15 pF,	R _L = 400 Ω	10	16	25	ns
tpd0	Propagation delay time to logical 0 level from clock to output	69	C _L = 15 pF,	RL = 400 Ω	10	25	40	ns

SIZE SYMBOL DRAWING NO.

A B < 3008BZ SHEET 6 OF 6 SCALE:

[‡]All typical values are et $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$. § Not more than one output should be shorted at a time.

	REVISIONS			
LTF	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PERECH 3203		3/8/70	M.J.C

	REV STATUS	REV	A	A														
Į	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	TOLERANCES UNLESS OTHERWISE S DECIMAL DIMENSION ANGLES	PECIFIED	DRAWN 11.17.0EN DRAFTING	YSY_	IK'D		ATE.	Abbassinasaa	ALMMINISTER NO	30F			THE BORO,				PANY TS, U	.S.A.
								D	IRC JYE	UIT	N-L	ITE ITE	巴平	ACK	DAGE	-		
1	SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	LOCAL A		200	-4/	15/~.	SIZE		P	>				/ING			
	DESIGNED FOR		CORPORAT RELEASE	re S. Fig.	AUKLI	a V	j Vices	SCAL				W	Τ	SH	EET	1 (OF 2.	
	EDDN 6350 C IEVO							A										

DESCRIPTION

Circuit, Integrated 4 line to 10 line decoder

2. PHYSICAL CHARACTERISTICS

2.1 16 pin dual in-line package.

For more detailed physical characteristics, see mfg.'s catalog.

3. PERFORMANCE CHARACTERISTICS

- 3.1 Supply voltage Vcc 4.75V to 5.25V
- 3.2 Fan out 10 unit loads
- 3.3 Ambient temperature 0°C to 70°C

For more detailed performance characteristics, see mfg.'s catalog.

4. QUALITY ASSURANCE PROVISIONS

Inspect per parameter outlined in mfg.'s catalog.

5. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, or Engineering approved equivalent.

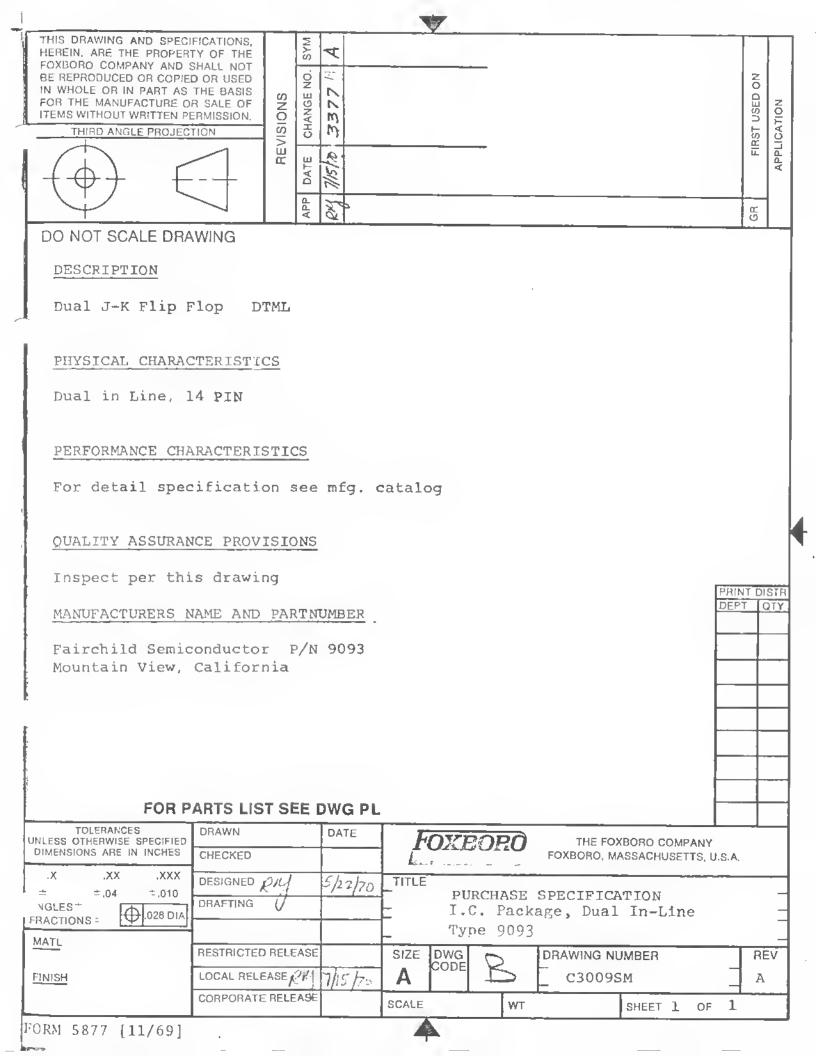
Part No. SN7442

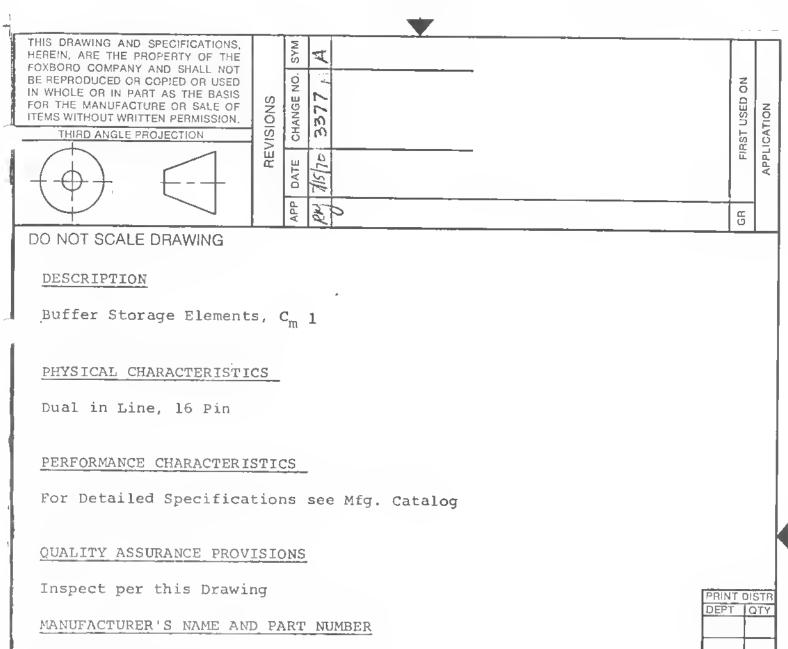
NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

A B CBOSEL A

SCALE: SHEET 14.0F7

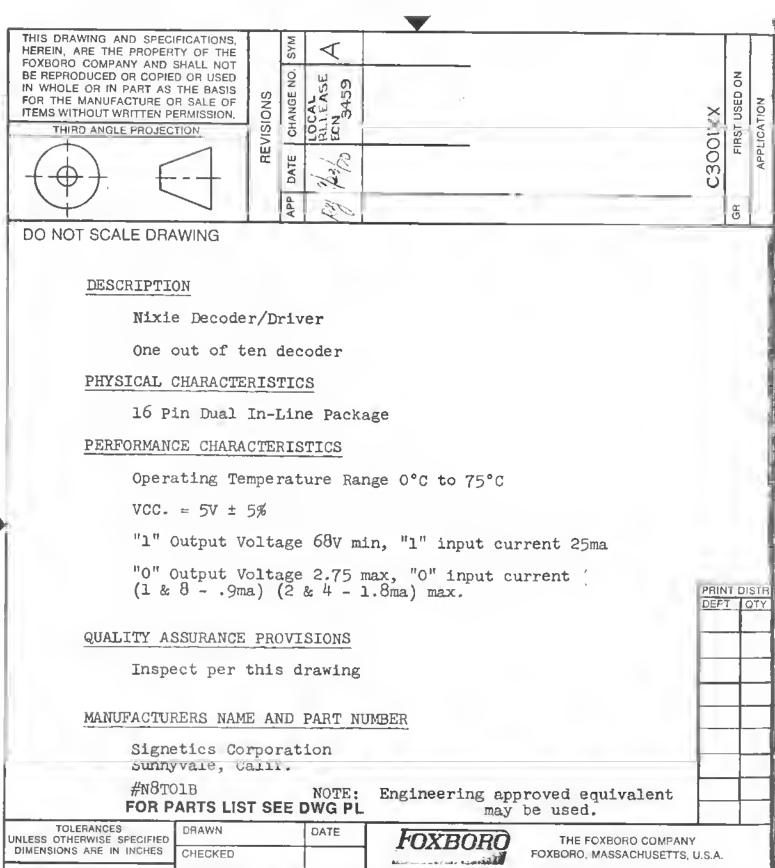




Fairchild Semiconductor P/N 9959 Mountain View, Cal.

FOR P	ARTS LIST SEE	OWG PL			
TOLERANCES UNLESS OTHERWISE SPECIFIED	DRAWN	DATE	FOXBORO	THE FOXBORO COMPANY	
DIMENSIONS ARE IN INCHES	CHECKED		E	FOXBORO, MASSACHUSETTS, U.S.A.	
.X .XX .XXX ± = .04 = .010 NGLES+ FRACTIONS = .028 DIA MATL	DESIGNED PM DRAFTING	5/12/70		SE SPECIFICATION ackage, Dual In-Line 959	
	RESTRICTED RELEASE		SIZE DWG	DRAWING NUMBER	REV
FINISH	LOCAL RELEASE RW	1/15/10	A	C3009SS	Α
	CORPORATE RELEASE		SCALE W1	SHEET 1 OF 1	

FORM 5877 [11/69]



	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
	LOCAL REIEASE PER ECN # 4057		2/13/20	mydak

1						_				_								
	REV STATUS	REV	1.						<i>L</i> .									
	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	TOLERANCES UNLESS OTHERWISE S DECIMAL DIMENSION ANGLES	SPECIFIED	DRAWN DRAFTING		HK'D	D/	ATE	FO	XI	3 <i>OF</i>	10		THE BORO,				PANY TS, L	.S.A.
	ANGLES ± 1°		DESIGNED	14.	1 1	7	10				•		TITLE					
1								DUA L-	-JN~	LENE	PA(CYAG:	E I.	C. I	EC :	CYPE	380	Α
	SUPERSEDING INTERCHANGEABLE YES SIMILAR TO NO		APPROVED LOCAL RELEASE	36.1	1.1	14 121	, 1.	SIZE DRAWING NU B C3313AA						NUM	BER			
	DESIGNED FOR FOX		CORPORAT RELEASE			_	3/72					W	Т	SH	EET	! (DF _	-
								A										

DESCRIPTION

Dual-In-Line Package, I.C. DEC Type 380A

QUAD, 2 Input-Nor

PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin (See sheet #3 Must withstard soldering temperature with no deformation.

PERFORMANCE CHARACTERISTICS

Supply Voltage: 5.5 Volts Continuous (ase note 1)
Input Voltage: 5.5 Volts (see note 1 and 2)
Recommended Operating Conditions: 4.75 to 5.25 Volts
Storage Temperature Range: - 55°C to 125°C

Notes: 1. Voltage values are with respect to network ground terminal

2. Input signals must be zero or positive with respect to network ground terminal.

QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

MANUFACTURER'S NAME AND PART NUMBER

Digital Equipment Corporation 146 Main Street Maynard, Masa.

P/N 19-09705 (DEC TYPE 38QA

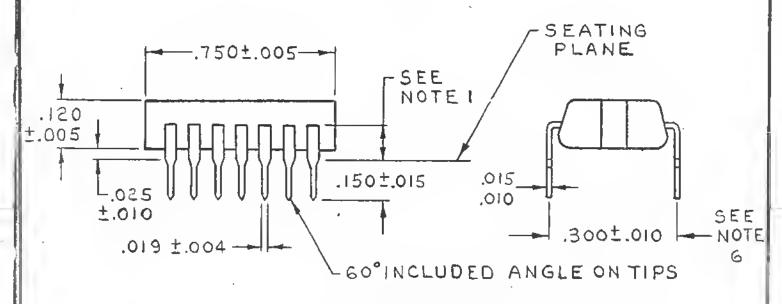
OR EQUIVALENT FROM QUALIFIED VENDOR WHO MEETS SPECIFICATIONS

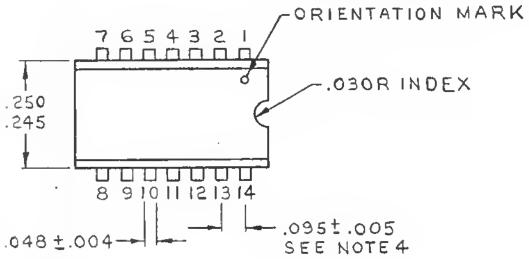
SIZE SYMBOL DRAWING NO.

A B C3313AA A

SCALE: SHEET 2 OF

DO NOT SCALE PRINT





NOTES:

- 1. Lead spacing shall be measured within this zone.
- 2. Molded plastic body.
- Kovar Leads
- 4. Lead spacing tolerances are non-cumulative
- 5. Thermal resistance from junction to still gir. J-A-C.16° C/M
- 6. Dimensions while inserted in carrier per DEC SPEC 19 00000 00

SIZE SYMBOL DRAWING NO.

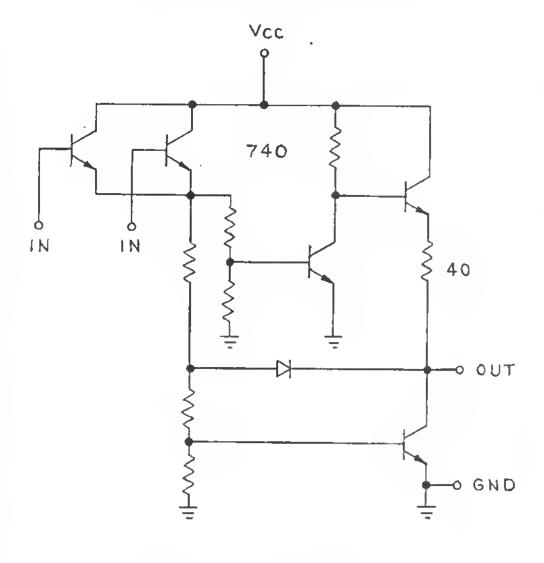
A B C C 3313 A A A

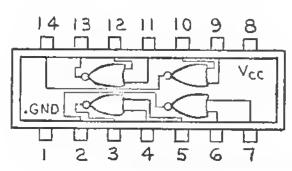
SCALE: SHEET 3 OF

DO NOT SCALE PRINT

FORM A818 - 088-4/68

CIRCUIT SCHEMATIC (4 OF CIRCUIT SHOWN)





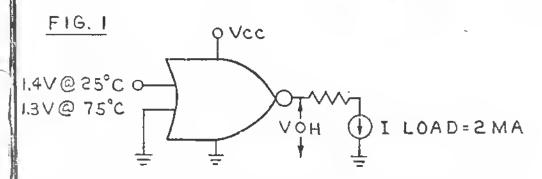
SIZE SYMBOL DRAWING NO. REV

A B C C 3 3 1 3 A A A

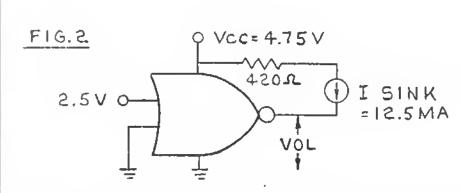
SCALE: SHEET 4 F

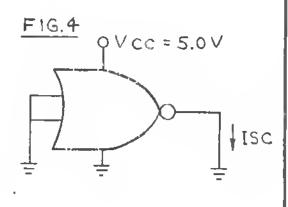
DO NOT SCALE PRINT

FORM ABIR-088-4/85

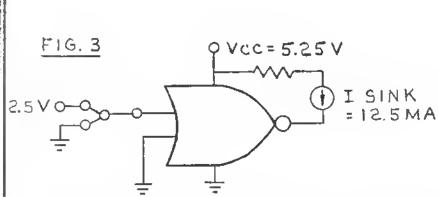


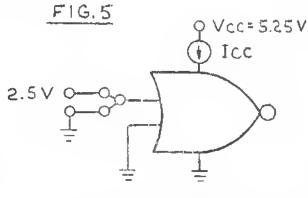
I. EACH INPUT TESTED SEPARATELY





2. EACH INPUT TESTED SEPARATELY





TEST ALL FOUR GATES
SIMULTANEOUSLY

3. EACH INPUT TESTED SEPARATELY

SIZE SYMBOL DRAWING NO.

A B C3313AA A

SCALE: SHEET 5 OF

DO NOT SCALE PRINT

FORM ABIS-088-4/88

BLECTRICAL CHARACTERISTICS, TA=0°C	2 to 75°C	5)			
	TEST FIGURE	TEST CONDITIONS	MIN.	MAX.	TIND
1. VoH Output High Voltage	П	Vcc: 4.75 V	3.5		Δ
2. Voleout Low Voltage	Ŋ	Vcc: 4.75 V		9.0	Λ
3. VIH Input High Voltage	Ø	Vcc: 4.75 V	2.5		Λ
4. VIL Input Low Voltage	Ħ	Vcc: 5.25 v		1.40 25°C 1.30 75°C	Λ
5. IH Input High Current	M	Vcc: 5.25 V	•	160	AA
6. IL Input Low Current	m	Vcc: 5.25 v		-25	A.A.
7. ISC Output Short Circuit Current	77	Vcc: 5.0 V	-30	-100	MA
8. Icc Supply Current (VIL)	Ŋ	Vcc: 5.25 V		Ø	MA
9. ^I CC Supply Current (^V IH)	ш	Vcc: 5.25 V		. 50	MA
SHALL BE CAPABLE OF MEETING SWITCHING		CHARACTERISTICS, TA =	0,0	15°C	
10. TPD & Positive Trigger Input TO Output Leading Edge 6		Vcc: 5.0 V CL: 15 PF CL: 50 PF	10	84 707	NS
11. TPD 1 Negative Trigger Input To Output Trailing Edge 6		VCC: 5.0 V CL: 15 PF CL: 50 PF	100	45 50	SSS

SIZE SYMBOL ORAWING NO.

A B C C 3 3 1 3 A A STATE STATE SHEET 7 OF 7

DO NOT SCALE PRINT

FORM A818-088-4/88

	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
1	LOCAL RELEASE PER ECN # 4057		2/13/72	m/Cook

1												_						
	REV STATUS	REV	A					A										
	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	TOLERANCES UNLESS OTHERWISE S DECIMAL DIMENSION ANGLES	PECIFIED	DRAFTING		HK'D	D	ATE			3OF			THE BORO,				PANY TS, U	.S.A.
			DESIGNED	//	10		2/7/					· · ·	TITLE					
1				1				DUAL	-IN-	LINE	Z PA	CKAG	E I.	C. 1	DEC '	TYPE	888	1
ı	SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	LOCAL RELEASE	10.	3/) . 3/	% (*) Z	SIZE		B				ORAW (313/		MUM	BER	
	DESIGNED FOR FOX	-2	CORPORAT RELEASE	E 3, FR	ANKL	N 6/2	elv:	SCALI				W	Т	SH	EET !		DF (

DESCRIPTION Dual-In-Line Package I. C. DEC Type 8881

QUAD, 2 Input Nand, Open Collector.

PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin (See sheet #3) Must withstand soldering temperature with no deformation.

PERFORMANCE CHARACTERISTICS

Supply Voltage:

Input Voltage:

7 Volts (see note 1)
5.5 Volts(see note 1 and 2)

Recommended Operating Condition: 4.75 Min. to 5.25 Volta Max.

Operating Free-air Temperature Range: 0°C to 70°C

Storage Temperature Range: - 55°C to 125°C

Note 1. Voltage values are with respect to network ground terminal.

2. Input signals must be zero or positive with respect to network ground terminal.

QUALITY ASSURANCE PROVISIONS:

Inspect per this drawing.

MANUFACTURER'S HAME AND PART NUMBER

Digital Equipment Corporation 146 Main Street Maynard, Mass.

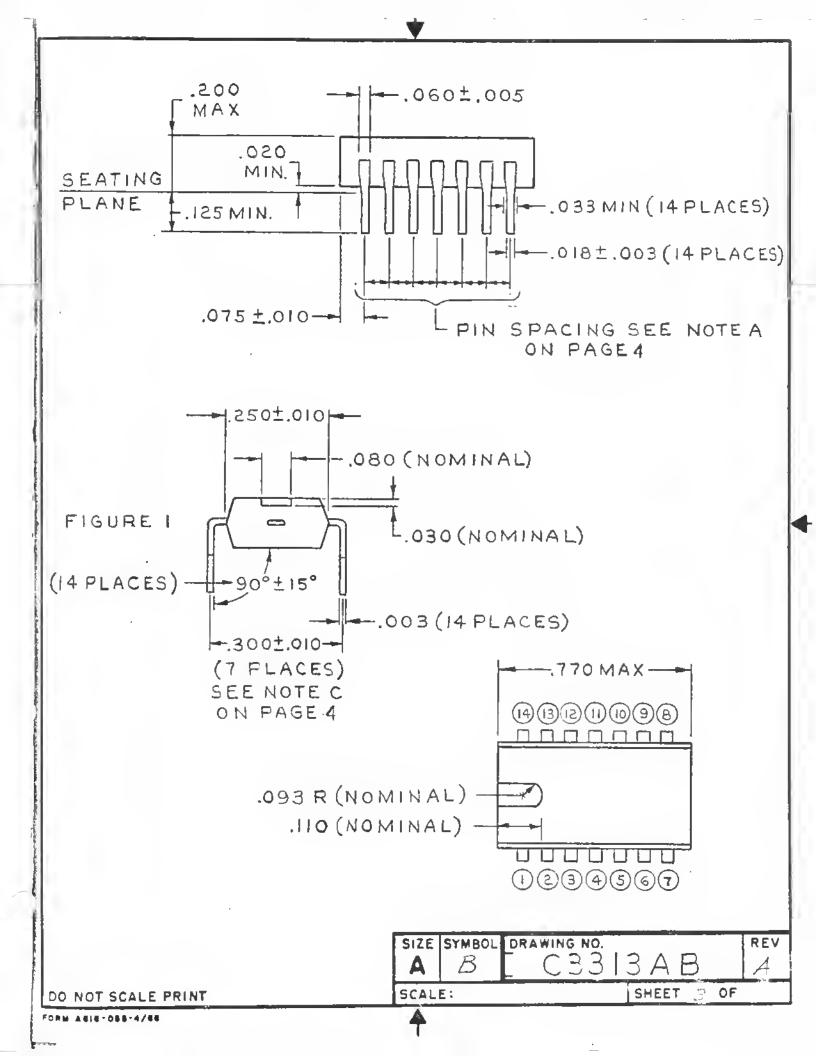
P/N 19-09705 (DEC TYPE 8881

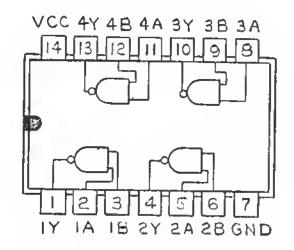
OR EQUIVALENT FROM QUALIFIED VENDOR WHO MEETS SPECIFICATIONS

> SIZE SYMBOL DRAWING NO. REV 24 C3313AB SCALE: SHEET 2

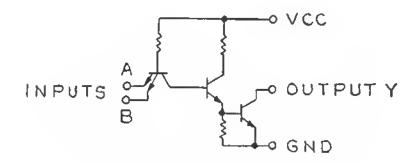
DO NOT SCALE PRINT

FORM A616-088-4/68





POSITIVE LOGIC Y= AB



SCHEMATIC (EACH GATE)

- NOTES: A. The True-position pin spacing is 0.100 between centerlines. Each pin center-line is located within ±0.010 of its true longitudinal position relative to pin 1 and 14.
 - B. All dimensions in inches unless otherwise noted.
 - C. Dimensions while inserted in carrier per DEC Spec. 19-00000-00.

SIZE SYMBOL DRAWING NO.

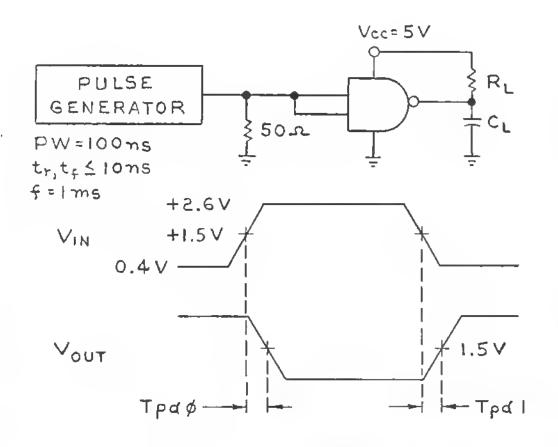
A B C C 3 3 | 3 A B A

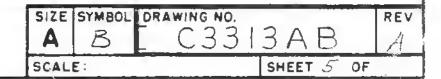
SCALE: SHEET # DF

DO NOT SCALE PRINT

FORM A818-088-4/68

PARAME	TER	TEST CONDITIONS (Figure 1)	MIN.	TYP.	MONIC.	TYPE
T _{PD} Ø	Propagation delay time to logical 0 level	$R_{L} = 100$ $C_{L} = 15$ PF			25	ns
T _{PD} 1	Propagation delay time to logical l level	$R_L = 3.9 \text{ KIL} - \text{OHMS}$ $C_L = 15 \text{ PF}$			35	NS





ELECTRICAL CHARACTERISTICS, TA = .	= .0°C to 70°C				
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	MAX. UNTES
VIW(1) Logical linput voltage required at all input terminals to ensure logical Q (OR) level at output.		2.0			>
VIN(0) Logical O input voltage required at any input terminal to ensure logical 1 (OFF) level at output.	$^{V_{GC}} = 4.75 \text{ V}$			0,8	>
IoUT(1) Output Reverse Current	$^{V}_{CC} = 4.75$, $^{V}_{IN} = 0.8v$ $^{V}_{OUT} (1) = 3.5 v$			25	μA
Vour(0) Logical O output voltage (Test 1)	$^{\text{V}_{\text{CC}}} = 4.75$, $^{\text{V}_{\text{IN}}} = 2 \text{ V}$, $^{\text{I}_{\text{SIMK}}} = 50 \text{ MA}$			0.8	>
Vour(0) Logical O output voltage (Test 2)	$^{V_{CC}} = 4.75, ^{V_{IN}} = 2 \text{ V},$ $^{I_{SINK}} = 16 \text{ MA}.$			ካ • 0	>
IIN (0) Logical O Level Input Current Each Input	VCC = 5.25, VIN = 0.4 V			-1.6	MA
<pre>ICG (0) Logical 0 Level Supply Current</pre>	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 5 \text{ V}$			55	MA
<pre>ICC (1) Logical 1 Level Supply Current</pre>	$V_{CC} = 5.25 \text{ V}$, $V_{IN} = 0$			35	MA

SIZE SYMBOL DRAWING NO.

A B C C 3 3 1 3 A B 4

SCALE: SHEET 6 OF 6

DO NOT SCALE PRINT

TORM A818-088-4/88

	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	Local Release ECN Number 3982		29 CCT 71	Keyr
B	ECN NO. 4102		10 APR 72	KCHT

							_											
	REV STATUS	REV	A	А	Α	Α	А	А	_									
	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	TOLERANCES UNLESS OTHERWISE S DECIMAL DIMENSION ANGLES	PECIFIED	DRAWN P FYLL DRAFTING	14	łK'D	0	ATE			30F			THE S					J.S.A.
1			DESIGNED E . H	ERE	27			(irc Pack	uit, age	Int Typ	tegra	TITLE ated N 74	. Dua	1R Ir	ı-Li	ne	
1	SUPERSEDING INTERCHANGEABLE SIMILAR TO	` ,	1		000	SIZE		E	3			ORAW 3313	VING AC	NUM	BER			
DESIGNED FOR CORPORATE RELEASE SCALE WT SHEET								} (OF G	>								
	0014 5750 0 464401							A										

1.0 DESCRIPTION

Hex Buffers/Drivers with open-collector, high-voltage outputs.

2.0 PHYSICAL CHARACTERISTICS

14-Pin Plastic Dual-In-Line package (N Type). Shall be marked with mfg.'s type no.

3.0 PERFORMANCE CHARACTERISTICS

Shall be per Table 1.

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments, Inc. Dallas, Texas P/N SN7407

Or Equivalent from qualified vendor who meets specifications.

SIZE SYMBOL DRAWING NO.

A B C3313AC B

SCALE: SHEET 2 OF 6

TABLE 1
RECOMMENDED OPERATING CONDITION

	MIN.	NOM.	MAX.	TINU
Supply Voltage -VCC Output Voltage -VOH	4.75	•5	5.25 30	v
Low-Level Output Current, IOL Operating free-air temperature range TA	0	25	40 70	MA C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted).

Parameter	Test * Conditions	MIN.	MAX.	UNIT
VIH-High-Level Input Voltage VIL-Low-Level Input Voltage IOH High-Level Output Current	VCC=MTN VT_2V	2	0.8	V V
n-B- B-+-2 Output Outfolio	VOH=MAX		250	UA
VOL Low-Level Output Voltage	VCC=MIN.VI=0.8V IOL=16MA		0.4	V
IIH High-Level Input Current (Each Input)	VCC=MAX.VI=2.4V VCC=MAX.VI=5.5V		40 1	UA MA
IIH Low-Level Input Current (Each Input)	VCC=MAX.VI=0.4V		-1.6	MA
ICCH Supply Current, High- Level Output	VCC=MAX.VI=O	TYP** 29	41	MA
ICCL Supply Current, Low- Level Output	VCC=MAX.VI=O	TYP** 21	30	MA

SIZE	SYMBOL	DRAWING NO.				REV
Α	B	C3313AC				В
SCAL	Ε:		SHEET	3	OF	6

Switching Characteristics VCC-5V, TA-25 C

Paramo	eter	Test Condition	MIN.	TYP.	MAX.	UNIT
TPLH	Propagation Delay Time, Low-To-High- Level Output	CL=15PF, RL=110 OHMS		17	26	ns
TPHL	Propagation Delay Time, High-To-Low Level Output	CL=15PF, RL=110 OHMS		10	15	ns

^{*} NOTES: For conditions shown as max. or min., use the appropriate value specified under recommended operating conditions for the applicable device type.

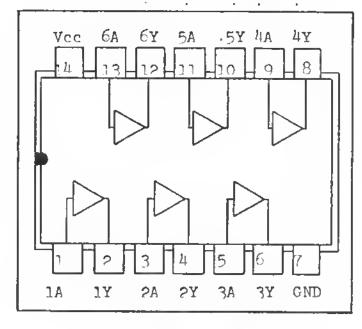
SIZE SYMBOL ORAWING NO.

A B C3313AC B

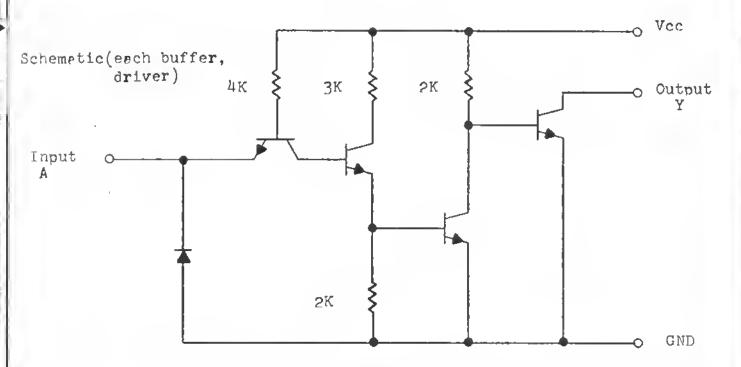
SCALE: SHEET 4 OF 6

^{**} All Typical values are at VCC - 5V, TA - 25°C

PIN DIAGRAM (TOP VIEW)



Positive Logic: Y= A

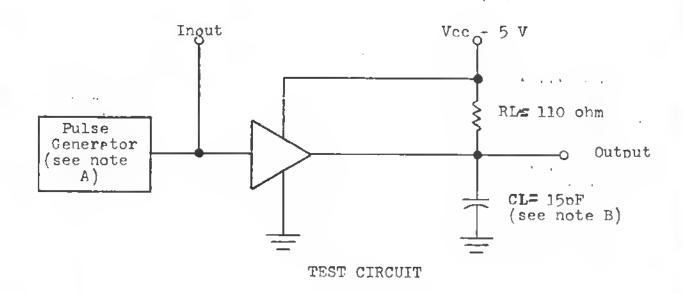


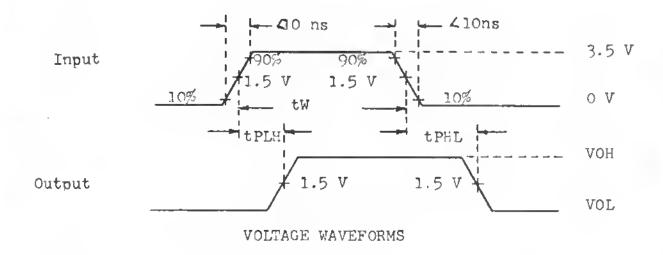
Note: Component values shown are norminal.

- 1	SIZE	SYMBOL	DRAWING NO.				REV
ł	A	B	C3313AC		В		
	SCAL	Ε:		SHEET	5	ζ.r	6

DO NOT SCALE PRINT

Switching characteristics





Notes:

- A. The generator has the following characteristics: tW-0.5us, PRR-1MH2, Z-out-50 ohms
- B.CL includes probe and jig capacitance

PROPAGATION DELAY TIMES

SIZE SYMBOL DRAWING NO.

A B C3333AC B

SCALE: SHEET 6 OF 6

DO NOT SCALE PRINT

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REVISIONS									
TŘ	DESCRIPTION		CODE	DATE	REVISED BY APPROVED BY				
4 LOCAL RE	LEASE PER ECN # 4057			2/13/22	29 Cor				
				Proposition for the control	A STATE OF THE PARTY OF THE PAR				

REV STATUS	REV	1,					Δ										
OF SHEETS -	SHEET	1	2	3	4	5	6	7	8_	9	10	11	12	13	14	15	16
TOLERANCES UNLESS OTHERWISE SPECIFIED DECIMAL DIMENSIONS ± .020 ANGLES ± 1°				HK'Ð	D/	ATE	FO)XI	30F	10	FOXE	THE BORO,					J. S. A.
ANGLES ± 1*		DESIGNED	L	7	,							TITLE					
							DU.	AL-1	[N-L]	INE	PACK	AGE	I.C.	SN'	74H7	8	
SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	LOCAL RELEASE	C.,	人人	5. V	$\frac{h_i}{2}$	SIZE		E	}		0331		/ING	NUM	BER	
DESIGNED FOR FO	x- 2	CORPORAL RELEASE 1	B, FR	ANKL	IN A	11472	SCALI	E			٧	/T	SH	EET	1 (DF	6

1.0 DESCRIPTION Duel-In-Line Package I. C. SN74H78 N

The J-K flip-flops ere besed on the master-slave principle. Inputa to the master section ere controlled by the clock pulse. The clock pulse elso reguletes the circuitry which connects the master end eleve sections.

2.0 PHYSICAL CHARACTERISTICS

Duel-In-Line 14 Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage:

Min.4.75 Volte Nom. 5.6 Volts Max. 5.25 Volts

Operating Free-Air Temp. Range: 0. to 70°CS Also see sheet # 3 and 4

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per thie drewing

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texes Instruments Incorporated Dallas, Texas. P/N SN74H78-N-

OR EQUIVALENT FROM QUALIFIED VENDOR WHO MEETS SPECIFICATIONS

1						
П	SIZE	SYMBOL	ORAWING NO.			REV
i	A	$\mid B \mid$	_ C 3313AD			A
1	SCAL	E:		SHEET	2_ OF	6

ELECTRICAL CHARACTERISTICS: (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE UNLESS OTHERWISE NOTED)

5 t 5 t t =	** ST CONDITIONS	MIN. T	YP: MAX.	UNIT
V-in(1) Input voltage required to ensure 1 at any input terminal	Voc # Min.	2		Volts
V-in(0) Input voltage required to ensure 0 at any input terminal	Voog Min.		0.8	Volts
V-out(1) logical 1 output voltage.	VccaMin. Iloada 500 uA	2.4		Volts
V-out(0) logical 0 output voltage.	Voc-Min. Isinkg20 mA		0.4	Volts
I-in(0) level input current at J or K	VccaMax. V-inm0.4 V		-2	mA
I-in(0) level input current at preset or clock	Voom Max. V-ingO.4 V		-4	mA
I-in(0) level input current at clear	Vcc= Max. V-in=0.4 V		-8	mA
I-in(1) logical (1) level input current at Jos at clear.	VoomMax, r K Vein 2.4 V VoomMax. Veinm5.5 V		50	II.2 UA
I-in(1) logical (1) level input current at preset or clock	VoomMax V-ing2.4 V VoomMax. V-ing5.5 V		100	mA uA mA
I-in (1) logical (1) level input current at clear	Voc=Max. V-in=2.4 V Vcc=Max. V-in=5.5		200	uA
Ios Short-circuit output current	VccsMax. V-inso. V	-40	-100	ma ma

SIZE SYMBOL DRAWING NO.

A B C3313AD REV

A

SCALE: SHEET 3 OF 6

DO NOT SCALE PRINT

ELECTRICAL CHARACTERISTICS CON'T

PARAMETER:	TEST CONDITIONS:	MIN.	* TYP:	MAX.	UNIT:
.Icc-Supply current	VoogMax.		÷32	50	mA

*-All typical values are at Vcc 5 V, TA 25°C
*** For conditions shown as Min. or Max. use the appropriate value specified under recommended operating conditions for the applicable device type.

	SWITCHING CHARACTERIST	ICS: Voc= 5 Vo	lts = 25°	N = 10	<u>)</u>
		CL = 25pF RL = 280 ohms	25 30		MHz
谷谷	ndl Propagation delay time to logical 1 level				
	from clear to output.	CL = 25pF RL = 280 o hms	6	13	ns
***	pd(0) Propogation delay time to logical 0 level from clear to output:	CL= 25pF RL = 280 ohm	12	24	ns
**	pd(1) Propagation delay time to logacal level from clock to output.	CL = 25pF RL = 280 ohm		5 21	ns
₩ ¥	pd (0) Propagation delay time to logical 0 level from clock to output.	CL = 25pF 280 oh		27	ns

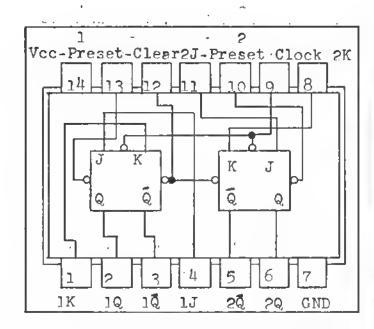
- ** NOT MORE THAN ONE OUTPUT SHOULD BE SHORTED AT A TIME, AND DURATION OF SHORT-CIRCUIT TEST SHOULD NOT EXCEED 1 SECOND.
- * FOR CONDITIONS SHOWN AS MAX.OR MIN, USE THE APPROPRIATE VALUE SPECIFIED UNDER RECOMMENDED OPERATING CONDITIONS FOR THE APPLICABLE DEVICE TYPE.

SIZE	SYMBOL	DRAWING NO. C3313AD			Ī	REV	
SCAL	E:		SHEET	1	OF	6	_

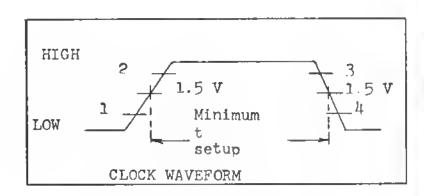
TRUTH	TABI	E
tn		tn+1
J	ĸ	Q.
0	0	Qn
0	· 1	0
1	0	-1
1	1	Qn

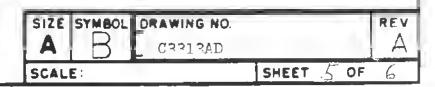
NOTES: 1. tn- Bit time before clock pulse,

tn+l- Bit time efter clock pulse.

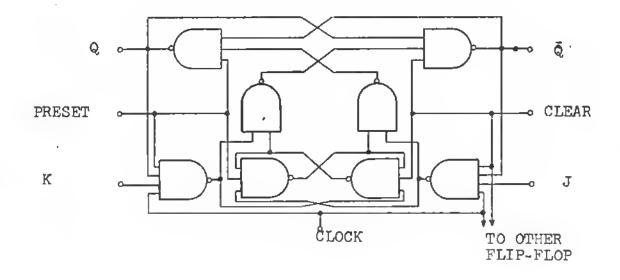


Positive Logic: Low input to preset sets Q to logical 1 Low input to clear sets Q to logical 0 Preset and clear are independent of clock

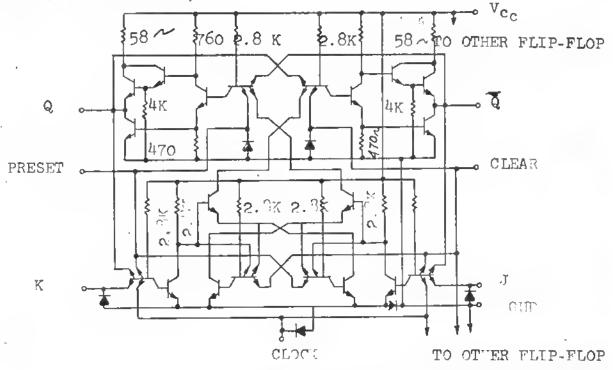




Functional block diagram (each flip-flop)



Schematic (each flip-flop)



SIZE SYMBOL ORAWING NO.

CR313AD

SCALE:

SHEET 6 OF 6

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		REVISIONS			
	LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
I	A	LOCAL RELEASE PER ECN # 4057		2/13/2	29cork

REV STATUS REV A A B A B B B B B B B B B B B B B B B							_											
TOLERANCES UNLESS OTHERWISE SPECIFIED DECIMAL DIMENSIONS ± .020 ANGLES DRAFTING DRAFTING DRAFTING DRAFTING DRAFTING DRAFTING DUAL—IN—LINE PACKAGE I.C. SN7486 SUPERSEDING INTERCHANGEABLE YES SIMILAR TO DIAL—IN—LINE PACKAGE I.C. SN7486 C3313AE C3313AE	REV STATUS	REV	A						A									
UNLESS OTHERWISE SPECIFIED DECIMAL DIMENSIONS ± .020 ANGLES DESIGNED DESIGNED DESIGNED DESIGNED DESIGNED DESIGNED DUAL—IN-LINE PACKAGE I.C. SW7486 SUPERSEDING INTERCHANGEABLE SIMILAR TO SIZE DRAWING NUMBER C3313AE C3313AE	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DUAL-IN-LINE PACKAGE I.C. SN7486 SUPERSEQUING INTERCHANGEABLE NO LOCAE SIMILAR TO DUAL-IN-LINE PACKAGE I.C. SN7486 C3313AE C3313AE	UNLESS OTHERWISE :	UNLESS OTHERWISE SPECIFIED DECIMAL DIMENSIONS ± .020 ANGLES ± 1° DRAFTING			нк'б	- 5	ATE					FOXE						
SUPERSEDING INTERCHANGEABLE VES NO LOCAE CORPORATE SIMILAR TO SIZE DRAWING NUMBER C3313AE C3313AE	ANGLES		DESIGNED	1/1	(+)\$	<i>f</i>							TITLE					
INTERCHANGEABLE YES NO LOCAE CONTROL OF A B C3313AE								DUA	L-II	N-LI	NE P	ACKA	GE I	.C.	SN7	486		
CORPORATE	INTERCHANGEABLE		LOCAE : (70	1	₹. 3/												
LECTIVE X RECEIVE DIT KHAKEINI AAAAA	DESIGNED FOR	x-2	CORPORAT	B.FR	MMKL	15] 14	เบ็นรั	SCAL	E			W	T	SH	EET	1	OF -	7

1.0 DESCRIPTION Dual-In-Line Package I.C. SN7486 N

Quadruple 2-input exclusive-or gatea. Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL oircuitry to perform the function: Y= AB +AB. When the input statea are complementary, the output goes to a logical 1.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage: 7 Volta
Input Voltage: (V in) 5.5 Volts (see note 1)
Operating free-air temp. Range: 0°C to 70°C
Storage Temp. Range: -65°C to 150°C

4.0 QUALITY ASSURANCE PROVISION

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments Incorporated Dallas, Texas. P/N SN7486-N

Note: 1. These voltage values are with respect to network ground terminal.

OR EQUIVALENT FROM QUALIFIED VENDOR WHO MEETS SPECIFICATIONS

SIZE SYMBOL ORAWING NO.

G3313AE

SCALE:

SHEET 2 OF 7

DO NOT SCALE PRINT

FORM ABIS: DEB-4/84

Electricel Characteristics Con't

Recommended operating conditions (over operating temp. Range) SN7486

						•
			$\underset{\cdot}{\text{Min}_{\bullet}}$.	Nom.	Max.	Unit.
	Supply Vol	tege Voc	4.75	5	5.25	Volts
	output N:	fen-out eech Logical O Logicel l	•		10.0 20.0	Volts Volts
	Operating :	free-eir temp. Renge	. 0		70.0	°C
	V in (1) V in (0)		2.0		0.8	Volts Volts
	V out (1)	Vcc = Min. V in (1) V in=(0) 0.8 V I load 800 uA	2.4			Volts
	▼ out (0)	Voc = Min. V in (1) 2 V V inc(0) 0.8 V			0,4	Volts
	I in (1)	Voc = Max. V in			40	uA
		2.4 V Vcc = Max. V in 5.5 V			1	mA
	I in (0)	Voc = Max. V in 0.4 V			-1.6	mA
Ķ-	103	Vco = Max. 4.5 V Vin = (0) 0		-18	-55	mA
	Icc	Voc = Max. V in:4.5 V		30	50	mA

** Note: Not more than one output should be shorted at a time.

SIZE	SYMBOL	DRAWING NO.			REV
A	B	_ 03313A	4		
SCAL	E:		SHEET 3	OF	1

Switching Characteristics: Vcc = 5 V TA = 25° C N 10

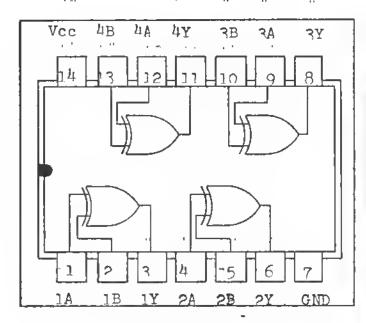
			-		
PARAMETER	TEST CONDITIONS	Min.	Тур.	Max.	Unit
tpd0	CL=15 pF RL=400 ohms	•	11	17	ns
tpdl	CL = 15 pF RL = 400 ohms	g de la companya de	15	23	ns
tpd 0	CL = 15 pF RL = 400 ohms		13	22	ns
tpd 1	CL=15 pF RL=400 ohms		18	30	ns

SIZE SYMBOL DRAWING NO.

A B C3313AE A

SCALE: SHEET 4 OF 7

TRUTH TABLE							
[nput:	2	outou	t.e				
Δ	В	v	ميد د				
0	n	0					
-0-							
. 0	1						
1	0	_1					
1	1	0					



Positive Logic: Y-A 0 B

SIZE SYMEDL ORAWING NO.

CREV

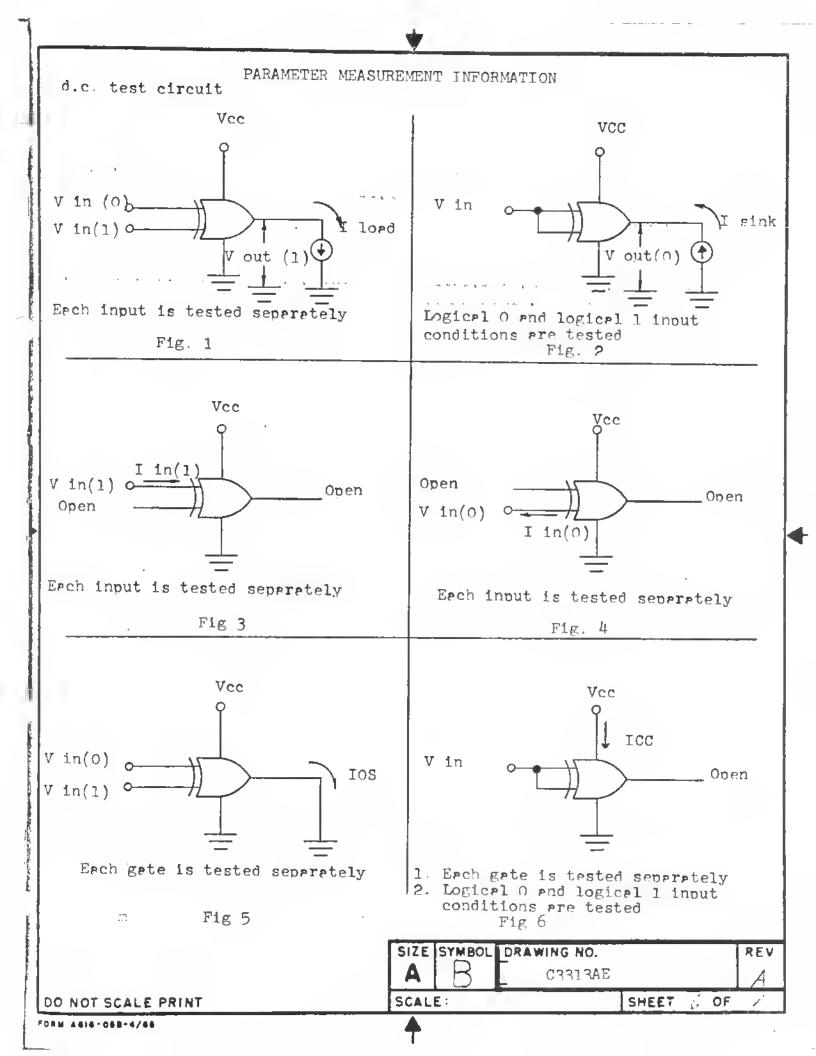
CREV

A

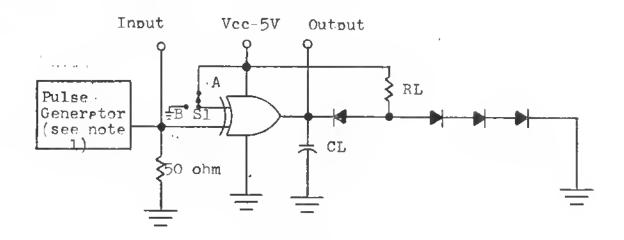
SCALE:

SHEET 5 OF 7

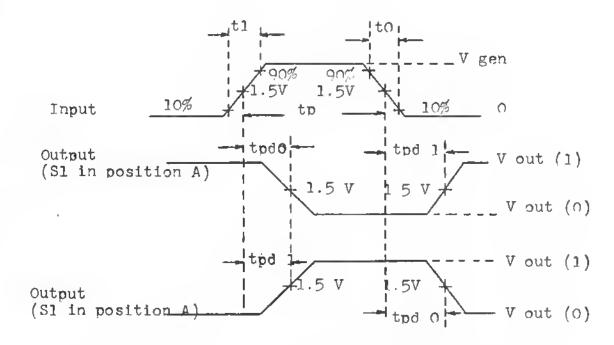
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Switching Characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

- 1. The generator has the following characteristics V gen- 3 V't o- t 1≤15ns tp-0.5 us PRR-1MHz ₹ Zout 50 ohm
- 2. All diodes are 1N3064
- 3. tpd0 +tpd1
- tpd-
- pd- 2 4. CL includes probe and jig_capacitance
- 5. Each gate tested separatol-

SIZE	SYMBOL	DRAWING NO.	· <u>-</u>		REV
Α	B	C33] 3AD			A
SCAL	E:		SHEET	7 OF	1

DO NOT SCALE PRINT

FORM A616-088-4/68

	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057		2/13/72	west

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REV STATUS	REV	A				1											
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
TOLERANCES UNLESS OTHERWISE DECIMAL DIMENSION ANGLES	SPECIFIED	DRAWN DRAFTING		HK'D	0	ATE	Annual Co.	Act of the later of the	BOR	10						PANY TS, L	J. S. A.
	DESIGNED		. 8,	15.71						TITLE							
							זם	JA L-	IN-I	LINE	PAC	KAGE	SN7	416	4		
SUPERSEDING INTERCHANGEABLE	YES	APPROVED	. '	, i			SIZE		П	}			DRAV		NUM	BER	
SIMILAR TO	N0 -	RELEASE/	YC	1.1	27	11	A			<u> </u>		C3313AF					
DESIGNED FOR FOX	-2	CDRPDRAT	B. Fr	RANKL	in n	UN TE	SCAL				W	π	SH	EET	/ (OF ,5	-

1.0 DESCRIPTION

8-Bit Parallel-Out Serial Shift Registers.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage: 5 Volts
Low-Level (Logical 0) Output Voltage: 0.2 Volts
High-Level (Logical 1) Output Voltage: 3.3 Volts
Noise Immunity: 1 Volt
Storage Temp. Range: 0°C to 70°C
Power Dissipation Typical: 180 Milliwatts
Maximum Input Clock frequency typical: 20 Megahertz

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments Dallas, Texas

P/N SN74164

OR EQUIVALENT FROM QUALIFIED VENDOR WHO MEETS SPECIFICATIONS

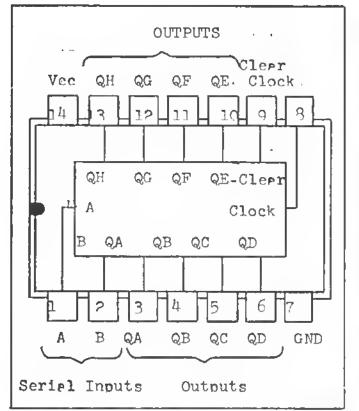
1	SIZE	SYMBOL	DRAWING NO.				REV
	A	B	C3313A1	?·			<i>A</i>
	SCAL	E :		SHEET	2	OF	ح ح

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FORM ABIS-088-4/68

SERIAL INPUTS A & B

TRUTT TA	ELE	
Inputs(tn	Output/th	-1)
H H L H H L L L	H L L H	



Positive logic: (see truth table)

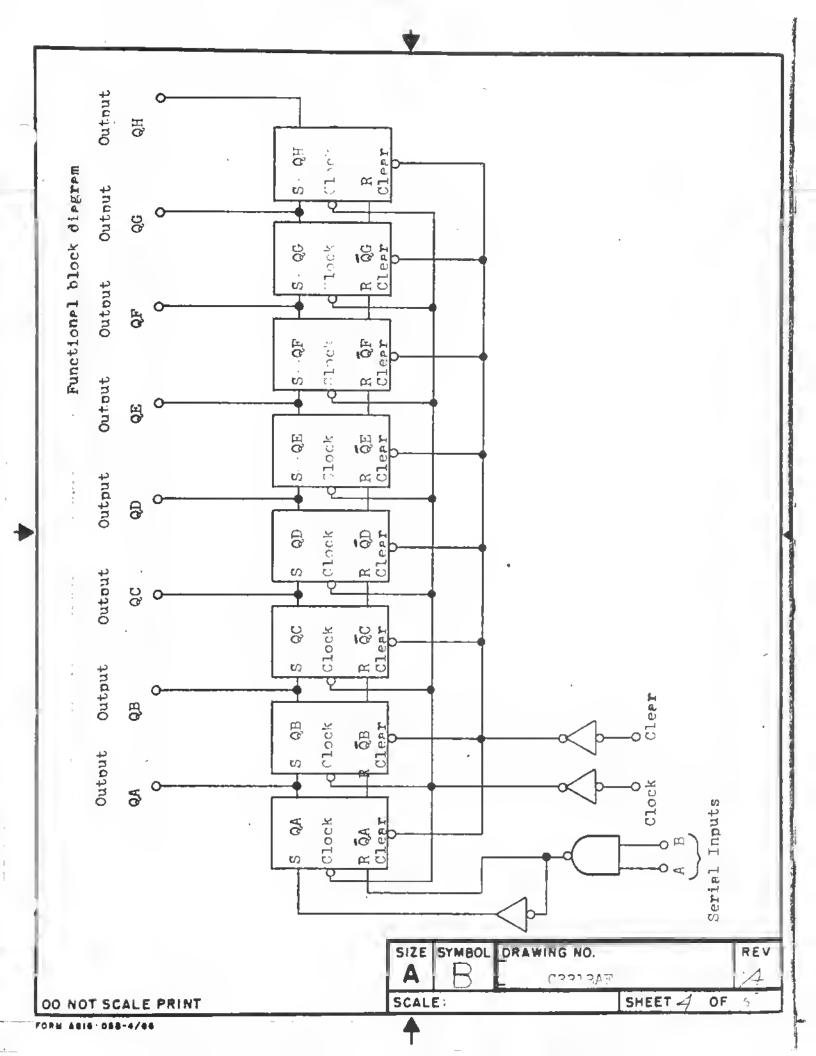
SIZE SYMBOL DRAWING NO. REV

A B C3313AF

SCALE: SHEET OF 5

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FORM A816-088-4/68



Typicel cleer.inhibit.shift.cleer. end inhibit sequences Clepr Clear 7 | 1 _____ Cleer Q. QB D, 8 QE. QH, 四 Ş Ø Outputs Seriel Inputs 1 4 1 4 SYMBOL DRAWING NO. SIZE REV CRRIPAF SCALE: SHEET DO NOT SCALE PRINT OF

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LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
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REV STATUS	REV						1				1						_
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
TOLERANCES UNLESS OTHERWISE DECIMAL DIMENSION ANGLES	SPECIFIED	DRAWN		HK'D		DATE	Fo)XI	POF	30					COMF HUSET	PANY TS, U	J. S. A
Andres.		DESIGNED	-							-		TITLE					
		Clerke	<i>J</i> ;	100 100	<u>~ 6</u>	[7]7 _.	DUA	L-II	N-LI	ne p	ACKA	GE :	L.G.	SN7	406		
SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	APPROVED LOCAL RELEASE	D				SIZE		,	جا	, (VING 3 A	NUM	BER	
DESIGNED FOR		CORPORA' RELEASE	TE		\neg		SCAL	Ē			W	<u>/Т</u>	SH	IEET	/ (OF /)	7

FDRM 5758-C (5/69)

1.0 DESCRIPTION Dual-In-Line Package I. C. SN7406 N

Hox Inverter, Buffers/drivers with open collector high voltage outputs. For interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays) and are also characterized for use as inverter buffers for driving TTL inputs.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin

11 1/2 1/2

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage: 7'Volts (See note 1)
Input Voltage: 5.5 Volts (See note 1)
Output Voltage: 30 Volts (See note 1 and 2
Operating free-air temp. range: -55°C to 125°C
Storage Temp. range: -65°C to 150°C
Also see sheet # 3 and # 4

4.0 QUALITY ASSURANCE PROVISION

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments Incorporated
Dallas, Texas. P/N SN7406-N

- Notes: 1. Voltage values are with respect to network ground terminal.
 - 2. This is the Max. voltage which should be applied to any output when it is in the off state.

SIZE	SYMBOL	DRAWING	NO.			REV
Α		[C33]	13A	\cdot		Α
SCAL	F:			SHEET	'2 OF	17

00 NOT SCALE PRINT

Electrical Characteristics: Contit

Recommended Operating Conditions

			SN7406		
		MIN.	NOM.	MAX.	UNIT
Supply Voltage	Voo	4.75	5	5.25	Volt
Output Voltage	V OH			30	Volt
	it Current, IOL			40	mA
Operating free-	air temperature range, TA	0	25	70	oc
PARAMETER	TEST CONDITIONS *	MIN.	TYP.	MAX.	UNI
VIH		2			Volts
VIL				0.8	Volts
ІОН	Vco = Min. Vl 0.8 V. VOH = Max.			250	uA
VOL	Voc = Min. Vl 2 V IOL = Max. 16 mA			0.7	Volts Volts
IIH	Vcc = Max. Vl 2.4 V Vcc = Max. Vl 5.5 V			40 1	uA mA
IIL	Voc = Max. Vl 0.4 V		d	-1.6	mA
IcoH	Voc = Max. Vl O		30	42	mA
IcoL	Voo = Max. Vl 5 V		27	38	mA -

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

** All typical values are at Vcc 5 V TA 25°C

SIZE	SYMBOL	DRAWING NO.			REV
Α	B	[C3313A	K C		A
SCAL	E:		SHEET 3	OF	17

OO NOT SCALE PRINT

^{*} For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

Switching Characteristics, Vcc 5 V TA 25°C

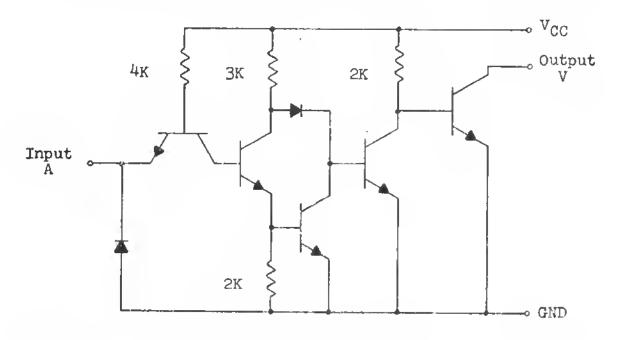
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
tPLH	CL = 15pF RL = 110 Ohms		17	26	ns
tphi.	CL = 15pF RL = 110 Ohms		13	20	ns

SIZE SYMBOL DRAWING NO.

A D C 3 13AG A

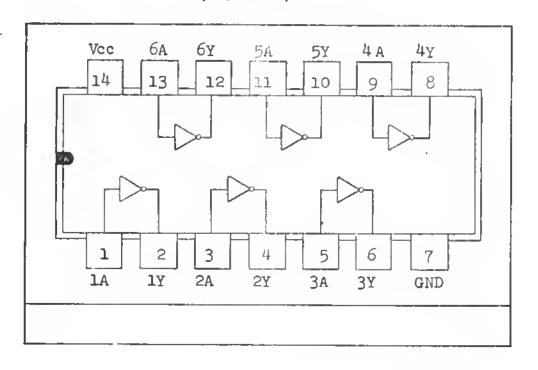
SCALE: SHEET 4 OF 17

Schematic (Each Inverter)



NOTE: Component values shown are nominal.

Jor N Dual-In-Line Package (Top View)



SIZE SYMBOL ORAWING NO.

C3313AG

SCALE:

SHEET 5 OF 7

OO NOT SCALE PRINT

PARAMETER MEASUREMENT INFORMATION

d-c test circuits

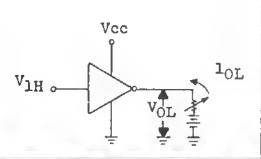


FIGURE 1 - V1H VOL

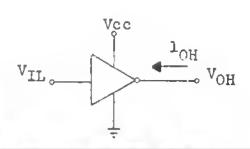


FIGURE 2 - VIL IOH

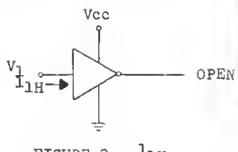
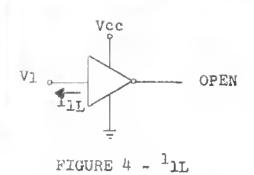
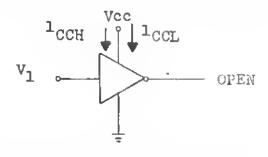


FIGURE 3 - 11H





All inverters are tested simultaneously.

FIGURE 5 - 1 CCH 1 CCL

Arrows indicate actual direction of current flow. Current into a termina is a positive value. SIZE SYMBOL! DRAWING NO. REV

SCALE:

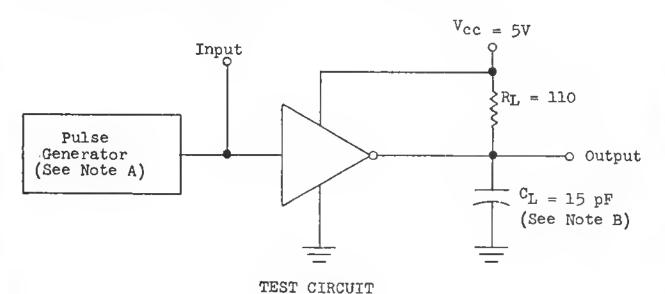
C3313AG

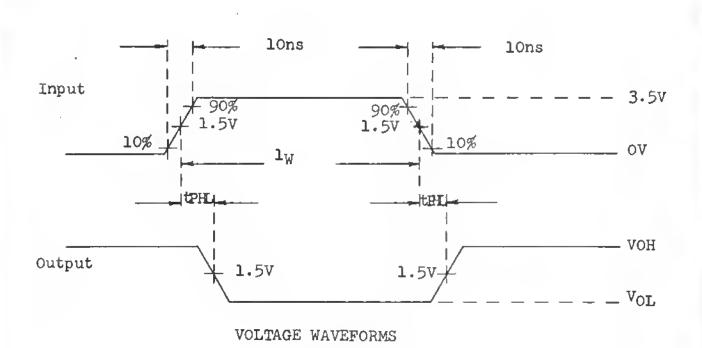
SHEET 6 OF

DO NOT SCALE PRINT

PARAMETER MEASUREMENT INFORMATION

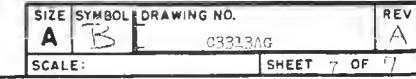
Switching Characteristics





NOTES: A. The generator has the following characteristics: tw=0.5 us, PRR=1 MHz, Zout = 50

B. CL includes probe and jig capacitance.



DO NOT SCALE PRINT

	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
$ _{\mathcal{A}} $	V) LOCAL RELEASE PER ECN # 4080		3/13/72	220

																	_
REV STATUS	REV	A	4				->	A									
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
TOLERANCE UNLESS OTHERWISE DECIMAL DIMENSION ANGLES	SPECIFIED	DRAWN	N	HKID M. G.V.L.	1 41	ATE LIVO.	- 10		3OA				_			PANY TS, U	
		DESIGNED	14	1.5	- 9/	20/7/					•	TITLE					
					+	\neg	DUAL.	-IN-	LINE	PA(CKAG:	E I.	c. s	N74:	17N		_
SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	APPROVED LOCAL RELEASE	roll.	<u>ت</u>	校	*/>1	SIZE		-	B			3313		NUM	BER	
DESIGNED FOR FOX-		CORPORA*	_				SCALE	i i	ONE		W	т	SH	EET	1 (OF	7

1.0 DESCRIPTION Dual-In-Line Package I.C. SN7417N Plastic-Pkg.

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high current loads. (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin Vendor P/N marked on case.

3.0 PERFORMANCE CHARACTERISTICS

See tablea #1. 2. 3.

Notea:

- (1) Voltage values are respect to network ground terminal.
- (2) This is the maximum voltage which should be applied to any output when it is the off state.

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments, Incorporated Dallas, Texas. P/N # SN7417

SIZE SYMBOL ORAWING NO.

C3313AH

SCALE: SHEET 2 OF 7

DO NOT SCALE PRINT

FORM ABIS-088-4/66

. Teble # 1

Recommended operating conditions

Supply Voltage VCC:	Min. Nom. 4.75 5	Mex. 5.25	Unit Volts
Output Voltage VOH:			
		15	Volts
Low-Level output current.	iol:	40	m.A
Operating free-air temp.Ra	enge: 0 25	70	°C

Table # 2

Flectrical characteristics over recommended operating free-air Temp. Range:

Parameter	test condition	Min.	Тур	Mex.	Unit.
VIH High-level input voltage:		2			Volts
VIL Low-level input voltage:				0.8	Volte
IOH High-level output current:	VCC=Min. V1- 2V VOH=Max.			250	uA
VOL Low-level output voltage	Vcc=Min Vl=0.8 VIOL=Mex.			0.7	Volts
	Vec-Min. V1=0.8 IOL-may.	V		0.4	Volts
IIH High-level input current (eac' input)	VCC-Mex. V1-2.4 VCC-Mex. V1-5.5	Ý.		40 1	uA mA

SIZE	SYMBOL	ORAWING NO.				REV
A	5	C3313AH	_			A
SCAL	E: N	ONE	SHEET	ニ	OF	7

Electrical Characteri Paramoter test	stics Table #2 Cont condition Min.	Typ.	Max.	Unit
IIL Low-level input current (each input)	Vcc-Max. Vl-0.4 V		-1.6	mA
ICCH Supply current high-level output	Voc-Mex. V1-5 V	29	41	mA
ICCL Supply current low-level output	Voc-Max. V1-0	21	30	mA

Switching Characteristics, Voc-5V TA-25°C

Table #3

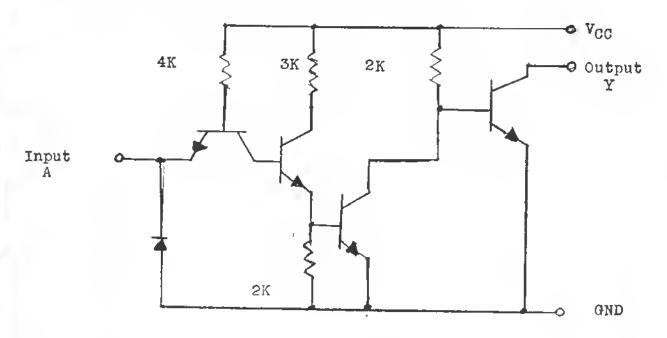
Parameter test	condition	Min.	Typ.	Max.	Unit.
delay time, low-to-	C _l = 15pF R _L = 110 Ohm		17	26	ns
trHL Propagation delay time, high-to-low-level output	C _L ± 15 pF R _{I.} = 110 Ohm		10	15	ns

SIZE SYMBOL DRAWING NO.

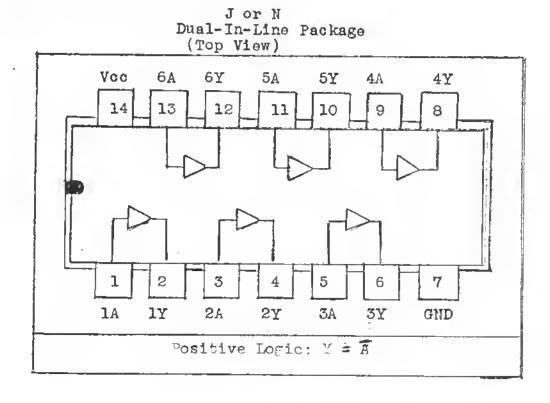
A C3313AH

SCALE: NONE SHEET 4 OF 7

Schematic (Each buffer/driver)

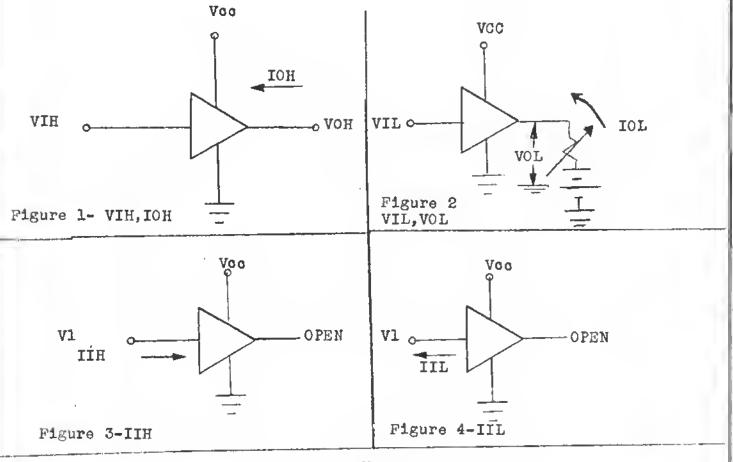


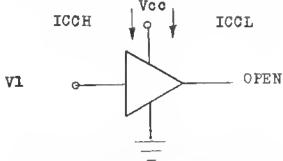
NOTE: Component values shown are norminal.



PARAMETER MEASUREMENT INFORMATION

d-c test circuit





All huffers/drivers are tested simultaneously.

FIGURE 5- I CCH 1 CCL Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

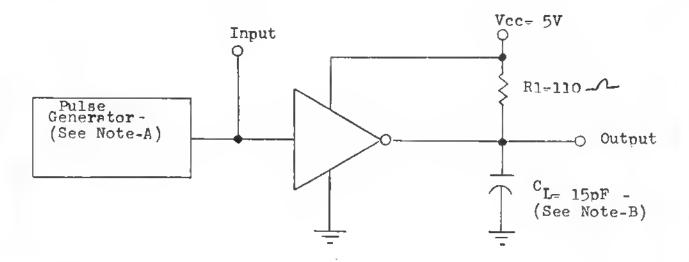
П	SIZE	SYMBOL	ORAWING NO.				REV	
- 6	A	D	_ 03313AH				A	
	SCAL	E: NUN	E	SHEET	b	ΟF	27	

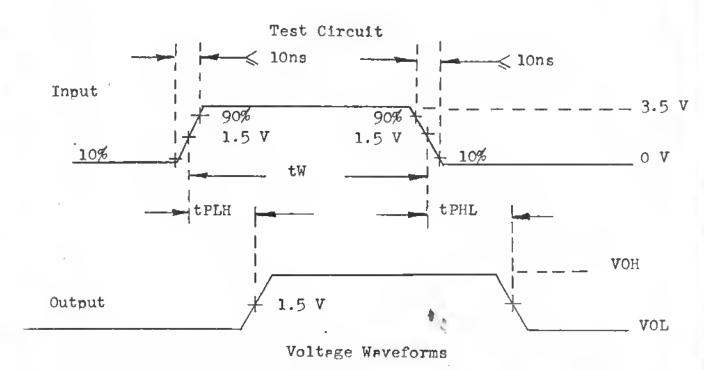
DO NOT SCALE PRINT

FORM ABIG-088-4/88

PARAMETER MEASUREMENT INFORMATION

Switching Cherecteristics





- Notes: (A) The generator has the following characteristics: tW= 0.5 us, PRR= 1 MHZ, Z out≈50 —
 - (B) CL includes probe and jig capacitance.



DO NOT SCALE PRINT

4

	REVISIONS	·		
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057		2/13/12	Mich

							_										
REV STATUS	REV	4	2	1													
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
TOLERANCES UNLESS OTHERWISE SPECIFIED DECIMAL DIMENSIONS ± .020 ANGLES TOLERANCES DRAWN - CHK'D DRAWN - CHK'D DRAWN - CHK'D				ATE)X1	BOF	? Q	FOXE				COMF	PANY TS, U	I. S. A.		
ANGLES ± 1*				!	<i>y</i>	2772		_	_		•	TITLE					
			•				DUA	L-I	N-LI	NE F	PACKA	GE S	SN74	37			
SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	APPROVE	h.	. 1 2 . L	7	, :/.	SIZE DRAWING NUMBER C3313AJ										
DESIGNED FOR FOX	-2	CORPORÁ RELEASE	H, FF	SHNKL	113 %	28/7:	SCALE				٧	/T	SH	EET	1	OF .	3

1.0 DESCRIPTION

Quadruple 2-Input Positive NAND Buffers SN7437

The NAND gate buffers feature very high fen-out capabilities (N-30).

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14-Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage: 5 Volts
Low Level (Logical 0) Output Voltage: 0.2 Volts
High-Level (Logical 1) Output Voltage: 3.3 Volts
Noise Immunity: 1 Volt
Storage Temp. Range: 0°C to 70°C

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments, Inc. Dallas, Texas

P/N SN7437

OR EQUIVALENT FROM QUALIFIED VENDOR WHO MEETS SPECIFICATIONS

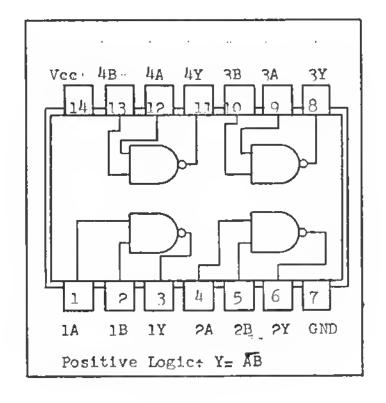
SIZE SYMBOL DRAWING NO.

A B C3313AJ

SCALE: SHEET 2 OF

DO NOT SCALE PRINT

FORM A818-088-4/66



SIZE SYMBOL DRAWING NO. REV

A B C3333AJ A

SCALE: SHEET 3 OF 3

DO NOT SCALE PRINT

FORM ABIR-088-4/48

F.W. LENS ALPRICATE BY DESCRIPTION COUL | DATE FAR SEPIA CHANGE F.S.P S. D. Gr. INDIC 1 ENGINE 1 2200 4 DATE 5056 72 1A-1 1A-1 1A-1 1A REV HOV STATUS GE SEDETS 10 15 5 9 11 12 16 2 | 3 13 14 SHEET Ó TO THE POST OF THE PROPERTY OF 174630 \$10KBSG 8.20 min 11 11 3 THE FOXEOUR COMPANY. D' AFTING FOXBORO, MASSACHUSETTS, U.S.A 6. Dron, Jan TITLE QUAD-Z INPUT OR GATE DRAWING NUMBER APPROVED and the same TI POBANGEABLE CSS13AI Latino Life and subsectivities / 07 5 137 W.E WI **ISBITT** William V

16.30

V 5758-C (5 69)

1.0 DESCRIPTION QUAC-2-Input, Positive OR GATE F.S.C.

PHYSICAL CHARLOTERISTICS

Dual-In-Line Package 14 Pin; FOR PIN ASSIGNMENTS

|A-1

3.0 FERFORMANCE CHARACTERISTICS

(Absolute Miximum Rating) See Notes 1, 2, 3, and 4

Voltage Applied: (All Terminals) #5.5 V #F.S.C.
IA-1

THE THE PROPERTY OF THE PARTY O

Temp. Operating Range: 0°0 to + 75°C - 65°C to + 150°C

4.0 QUALITY ASSUR HOR PROVISIONS
Inspect per this drawing

5.0 PARTHACTURER'S MAYO AND PART RUPPER

SIGNETICS, Corporation
Sit East Avoids Avoids (A Subsidiary of Corning Glass Works)
P/N # SP384A

SIZO LOYNOOL CHENNING NO. 1000

CA OT SCALE PRINT

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LOWER FOR

CHIMPERICAL CHARACTERISTICS: SPE NOTES 1, 2, 3, 5, and 7

STANDARD CONDITIONS: VCC- 5.0V TA-OPERATING TEMP. RANGE (UNLESS NOTED).

 $\mathbb{C}^{l_{1}}$

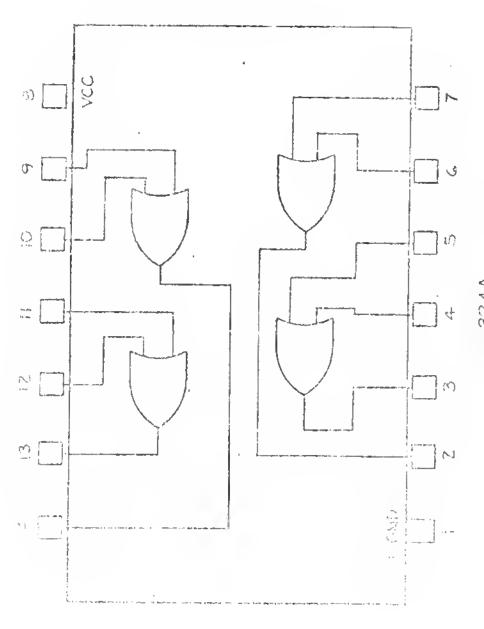
OVER COMMISSIOS	TEST CONDITIONS	HIN	TYI)	$\chi L_{\rm eff}$	full()
Koles Hamming	See note #6	1100	1700		MV
For "O"	See note #6	600	1000		MV
Output Voltage					
"O" F.S.C.	I-Out= 2 ml V-in= 2.7 V I-Out= 12.5 mA	3 .₽			v
114	V-in= 1.2V I-Out=7.5mA			0.6	V
	V-1n= 1.2v V	2		0.4	V
Input Current	74-	Ĩ			
Input Migh	V-in= 2.7V			180	uА
Power Supply Current	"/A-1				
Output High	V-ins4.0V		11.0	14.7	mš.
Cutput Low	V-in-0V TA-25°C		11.2	15.2	mA
Turn on Delay	Sce test Fig. 1	AZ)	50	80	ns
Turn off Delay	See test Fig, 1 TA= 25°C		40	70	ns
Fan-Out - to sink loads (B.da. 2 load)				5	
- to source loads (180M AMPS/LOAD)	E.S.C.			11	,

The state of the s	NAL BY
SINE ISTALLOCALINA NOTA NO.	TARY !
6 60010.T.	/A-
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100 P	5

D ROT SCALE PRINT

- (1). Firs not specifically referenced are left electrically opsite
- (2). All Valture resourcements are referenced to the ground plus
- (3). Positive Current flow is defined as current TWO the terminal indicated.
- (4). Precautionary massures should be taken to ensure current limiting per the maximum ratioss, should the isolation diedes become ferward blassd.
- (5). Fositive Logic definition: "Up level= "1" down level= "0",
- (6). This characteristics guaranteed by output measurements,
- (7). Manufacturor reserves the right to make design and process improvements.
- (8). Capicitance C includes probe and test jig.
- (9). For this test the signed input (Fin 2 or 13) is tied to +6V through ACK Ohm resistor.
- (10). Fin 14 must be tied to most negative voltage used.
- (11). Standard Source Load is 190uA and Standard Sink Load is +2.5mA.

1/A-



334A PIN CONFIGURATION

H BROSE

	REVISIONS			ì
LTR	DESCRIPTION	DR	DATE	APPROVED
A	LOCAL RELEASE		3JUL73	13-41 7

1. DESCRIPTION

FIRST USEO ON

Circuit, Integrated (Dual In-Line Package) CERAMIC Bual 4 Input Positive Nand "Power" Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

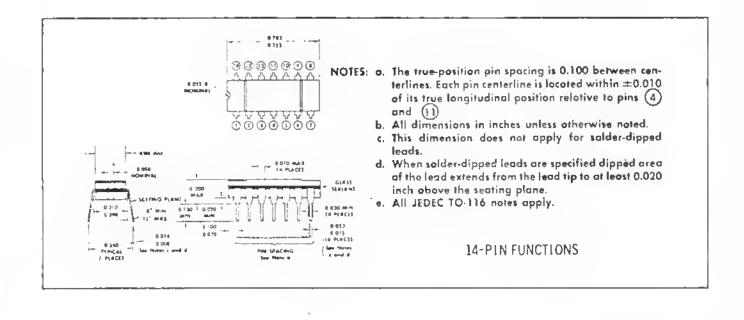
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7440J Sprague Part No. USN7440AJ SIGNETICS PART NO. N7440F Motorola Part No. MR7440L

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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HUERN OTHERWISE SPECIFIED	WORK AUTH NO.		ENERGY OF THE FO	XBORO COMPANY	
OVE BUNKS & BRARP COCCS. AG10NG ANG IN INCUES	DRAFTSMAN	PATE	FOXBORO, M	ASSACHUSETTS, U.S.A	۱.
THANCES ON	DESISHER	-	TITLE: CIRCUIT, INTEGRA		
.GTIONS. 2 1/64 DMALS 2 .CC5 CC0 12 1/2*	CHECKER:		DUAL IN-LINE PACE TYPE SN742		
MATERIAL!	ENGINGER		SIZE SYMBOL & DRAWING NO.	RE	V
FINISH: X	RELEASED		A B (3313A	P A	į
P	LOCAL RELEASE	<u> </u>	SCALE: NONE	SHEET I OF A	



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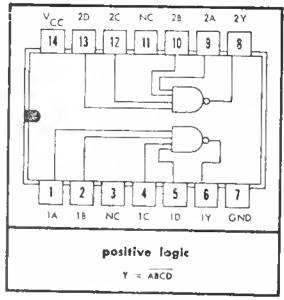
THE FOXBORO COMPANY SYSTEMS DIVISION

C3313AP

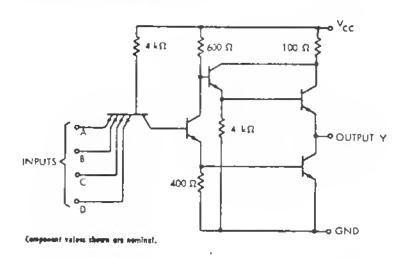
A

Rev.

\$N7440 J DUAL 4-INPUT POSITIVE NAND BUFFER



schematic (each gate)



THE FOXBORO COMPANY C3313AP

Sheet 3 of 4 A

recommended operating canditions

Supply Voltage V _{CC}																4.75	V to	5.2	25 5	1
fan-Out From Output,	N																	} to	3(3

electrical characteristics, $T_A = 0$ °C to 70°C

	PARAMETER	TEST FIGURE		TEST CO	NOITION	s	MIN	TYP	MAX	UNIT
V.0(1)	Lagical 1 input valtage required at all input terminals to ensure lagical 0 level at output	1	v _{ec} :-	475 V.	V _{out(0)}	< 04 V	2			v
١٨٥١	logical 0 input voltage required at any input terminal to ensure logical 1 level at autput	2	٧ _{cc}	475 V,	٧ _{٥٠1] ا}	· 24 V			0.8	٧
V _{out] ()}	Logical 1 output valtage	2	1.1.	475 V. -1 2 mA	Vie	0 H V,	2,4	3 3‡		٧
V _{au1[0]}	Lagreol D autput voltage	т .		4 75 V, 48 mA	٧,,,	2 V.		0 78‡	0.4	v
Leston	logical O level input current (each reput)	3	V _{CC}	5 25 V,	V,n	0 * V			-1.6	mA
I _{m(1)}	Logical 1 level input current (each input)	4		5 75 V. 5 75 V.	V.,,	2 4 V 5 5 V			40 1	μA mA
Los	Short circuit output current†	5	V _{cc}	5 25 V			- 18		-70	mA
10,010	Logical O level supply current (each gate)	6	Vcc	5 V.	٧,,,	5 V		861		mA
[Jeeld	Engical 1 level supply current (soch gate)	6	_vcc =	5 V.	٧,,,	0		2 1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25 \, ^{\circ}\text{C}$, N = 30

	TEST			1 1
PARAMETER	FIGURE	TEST CONDITIONS MIN	TYP MAX	TINU
I Prapagation delay time to logical O level	50	C _F = 15 pF	8 T3	[Re]
Ipd1 Propagation datay time to logical 1 level	50	$C_1 = 15 \text{ pF}$	18 29	n4

†Not more than one autput should be shorted at a time.

\$1here typical values are at $Y_{\rm CC}=5~V_{\rm c}~I_{\rm a}=25^{\rm a}{\rm C}_{\rm c}$

B

THE FOXBORO COMPANY SYSTEMS DIVISION

C3313AP

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Ray.

Shart & ac m

1. DESCRIPTION

FIRST USED ON

Circuit, Integrated (Dual In-Line Package CERAMIC)
Bual "B" Type flip Flop

 ∇

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 5
- 4. MANUFACTURER'S NAME AND PART NO.

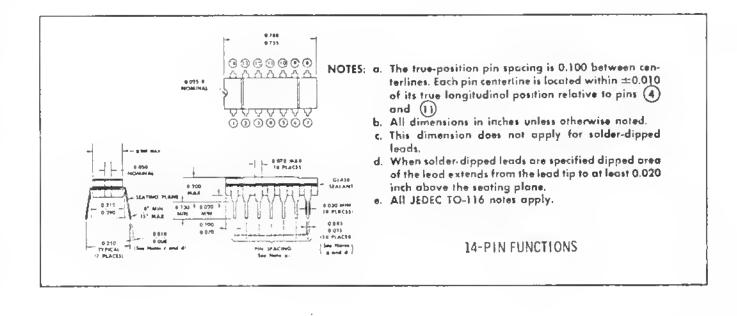
Texas Instrument, Part No. SN7474J Sprague Part No. USN7474.J

NOTE: Only the item described on this drawing when produced from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

E LEGS OTHERWISE SPECIFIED			THE FO	X BORO COMPANY
1 POVE BURRS & BHARPEDSES PRESMOTORS ARE IN INCHES	DRAFTEMAN	DATE		ASSACHUSETTS, U.S.A.
FOR LOADING APPLY AFTER PLATING	DESIRNER		TITLE: CIRCUIT, INTEGRA	
1 / CTIONS ± 1/64 (CIMALS ± .005	CHECKES.		DUAL IN-LINE PAC TYPE SN747	
NATERIAL: %	ENGINEER .		SIZE SYMBOL DRAWING NO.	ÎREV
FINISH:	MELEASO:	12/	A B C3313	AQ
	LOCAL RELEASE		SCALE: NONE	SHEET OF 5

5085A (8/67)



THE FOXBORO COMPANY SYSTEMS DIVISION

Rev.

2,05 Sheet

description

The SN7474 is a monolithic, dual, D-type, edge-triggered flip-flap featuring direct clear and preset inputs and complementary Q and \overline{Q} autputs. Input information is transferred to the Q autput on the positive edge of the clack pulse.

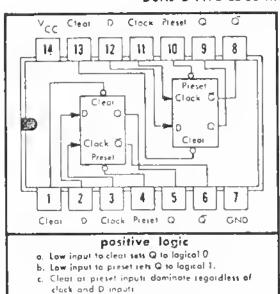
Clock triggering occurs at a valtage level of the clock pulse and it not directly related to the transition time of the positive going pulse. After the clock input shreshold voltage has been passed the data input (D) is lacked out.

The SN7474 dual flip-flap has the same clacking characterlistics as the SN7470 gared (edge-triggered) flip-flap and both are ideally twisted for medium, and high-speed applications. The SN7474 can be used at a rightficant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

Supply Voltage V _{CC}												4.7	5 V	to 5.25 V
Fan-Out From Each Output, N											٠			. 1 to 10
Width of Clack Pulse, Ipictock) (See Figure 56) .												٠		≥ 30 ns
Width of Preses Pulse, sp(plaint) (See Figure 53)														≥ 30 mi
Width of Clear Pulse, Iniciani (See Figure 53) .														≥ 30 ns

SN7474N DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



TRUTH TABLE (Each Flip-Flop)

10	" ₀ .	1
INPUT D	OUTPUT Q	OUTPUT
0	0	1
1	1	0

NOTES 1 $t_n = bit$ time below clack outse 2 $t_{n+1} = bit$ time often clack pulse.

THE FOXBORO COMPANY SYSTEMS DIVISION

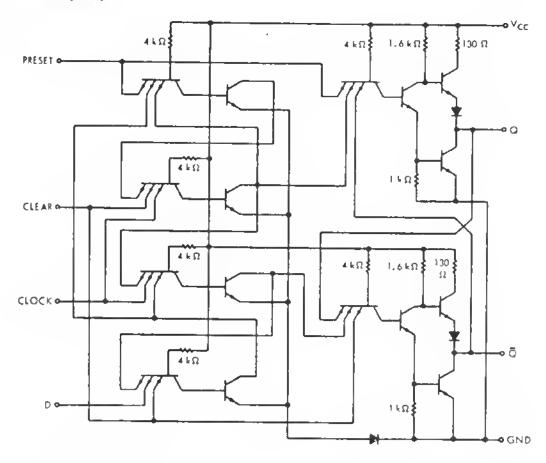
C3313AQ

Rev.

Sheet 3 of 5

Α

schematic (each flip-flop)



Component values shown are nominal,

THE FOXBORO COMPANY C3313AQ

Shoot 4 of 5

electrical characteristics, $T_A = 0$ °C to 70°C

	PARAMETER	TEST FIGURE	TES	T CONDITIONS	MIN	TYP	MAX	וואט
V _{ro(1)}	Input voltage required to ensure logical 1 at any input terminal	37	V _{CC} = 4.75 V		2			٧
V _{m(0)}	Input voltage required to ensure logical 0 of any input terminal	37	V _{CC} = 475 V				0.8	٧
V _{evi(I)}	Logical 1 output voltage	,37	V _{CC} = 475 V,	$I_{\rm road} = -400~\mu{\rm A}$	2.4	35‡		٧
V _{oul(0)}	Logical O output voltage	38	Y _{CC} = 4.75 V ₄	I _{trik} = 16 mA		0 22‡	0.4	٧
l _{in(0)}	Logical Q level input Current at preset or D	39	V _{CC} = 5.25 V _s	V _{rn} = 0.4 V			-1.6	mA
I _{in(0)}	togical O level input current of clear or rlack	39	V _{CC} = 5.25 V,	V _{sn} = 0.4 V			-3.2	mÅ
II _{In(1)}	Logical 1 level input	40	$V_{CC} = 5.25 V_{s}$ $V_{CC} = 5.25 V_{s}$	V _{.5} = 4.5 V V _{.5} ± 5.5 V			40	μA mA
l _{in(1)}	Logical Llevel input current of preset or clock	40	V _{CC} = 5.25 V. V _{CC} = 5.25 V.	V, - 24V V, - 55V		1	80	jiA mA
I ₁₀₍₁₎	Logicol 1 level input	40	$V_{CC} = 5.25 V_{i}$ $V_{CC} = 5.25 V_{i}$	V 74V V. 55V			120	μA
los	Short-circuit output current	41	V _{CC} = 5.25 V.	V, = 0	- 1B		-57	mA
Icc	Supply current (each flip-llop	40	V _{CC} = 5 V ₁	V ₁₀ = 5 V		8.5 ‡		mA

*Het mere then one output should be thatted at a lime,

switching characteristics, $V_{CC} = 5~V,~T_A = 25^{\circ}C,~N = 10$

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	וואט
Forock	Maximum clock frequency	56	$C_1 = 15 pF$	1.5	25		MHz
Letup	Minimum input setup time	56	C ₊ = 15 pF		15	20	กร
†hold	Minimum input hold time	56	C ₁ == 15 pf		2	5	F13
1 _{pd} I	Propagation delay time to logical I level from clear or preset to output	52	C, = 15 pF			25	ករ
1 _{pd0}	Propagation delay time to logical O level from risor or gretel to output	52	C ₁ = 15 pF			40	ns
† _{pd} r	Propagation delay time to logical I level from clock to output	56	C ₁ = 15 pF	10	20	35	ħΙ
† _{pd0}	Propagation delay time to logical O level from clock to output	56	$C_1 = 15 \text{ pF}$	10	28	50	775

THE FOXBORO COMPANY SYSTEMS DIVISION

C3313AQ

R∗..

Sheet 5 of 5

^{\$1}hsse typical values are at $Y_{CC} \sim 5 \ Y_c \ I_A = 25 \ ^oC$.

ON				REVISIONS			
	LTR		DESCRIPTION		DR	DATE	APPROVED
	A	LOCAL	RELEASE	:		3,000	a South of
		•		-			

1. DESCRIPTION

FIRST USED (

Circuit, Integrated (Dual In-Line Package CERAMIC)

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 4
- 4. MANUFACTURER'S NAME AND PART NO.

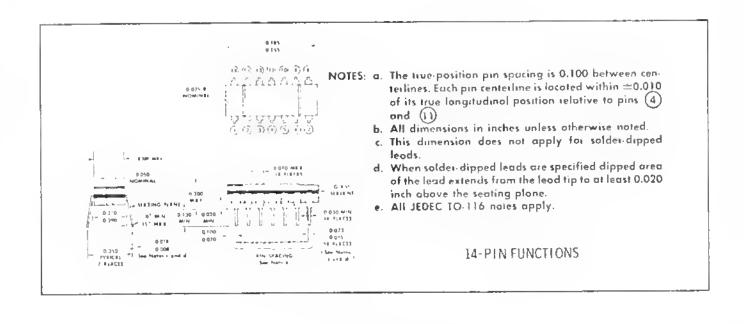
Texas Instrument, Part No. SN7405J SPRAGUE PART NO. US 7405J MOTOROLA PART NO. MC 7405L

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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FORWOVE BURRE & BHARP EDEZS FORWING ARE IN INCHES	OZAFTENAN .	DATE	A Carlon	Cast Pade Stage 1	FOXBORO, M	ASSACHUSETTS, C	J. S. A.
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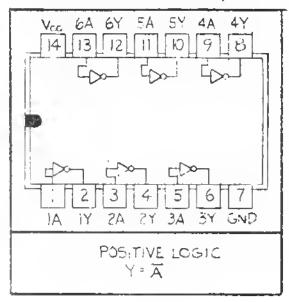
THE FOXBORO COMPANY SYSTEMS DIVISION

Sheet 2

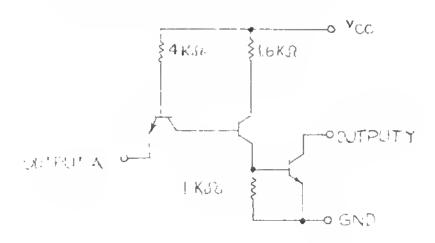
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Prim 5039 (6/68)

JORN DUALIN- LINE PACKAGE (TOP VIEW)



SCHEMATIC : EACH GATE)



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	DITIONS +			VBC : NI	IN S <	VIN: 0.4V	VEN : 2.4 V	>49. NEV	7 7 2 5	O "Z",
	TEST CONDITIONS +	N Z = 20 N	VCC = MIN	VCC = MIN,	CC - MIN ,		:		7.00-00	700 54
	TEC T FIGURE	15	16	16	,,,	1	ű		2.	92
	PAGAIVETER	V RESCRIPTION NOTAGE TWO TO ENSORE LOGICAL (OF) LEVEL AT THE	LOGICAL OLTAPLIT VOLTAGE FIG. 1. ATTAIN TERCONAL TO ENGURE LOGICAL I COPEN LEVEL AL TERROR	OUT(!) CUTPUT REVERSE CURRENT	SUT(O) LOGICAL O OCITRUTA VILLAGE (ON CENTRA)	INCO LOGICALC LE VER INPUT CURRENT	13 4 - 15 4 - 10 10 10 10 10 10 10 10 10 10 10 10 10	A. A	FCC(O) 10772A, C. 11 AEL SUPPLY CLIREFNIT	CC(1) CC. A L LEVE :

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CONDITIONS SAOW NIZO FEN OR MAX USE THE APPROPRIATE OFFICERED UNDER RECOMMENDED DEFINATING CONDITIONS NOTEST AND THORD DECK AS FER OR MAX APPLICABLE DEVICE TYPE, MILE YOU VALUE

TYFICAL VALUES ARE AT VCC = 5V, TA = 25°C # THESE

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SWITCHING CHARACTERISTICS, "CC = 5V, "A = 25°C

PARAMETER	7EST FIGURE	TEST CONDITIONS	MIN TYP- MAX UNIT
PRCHAGATION DELAY TO TIME TO LOGICAL Ø LEVEL	(n)	CL= 15PF, RL= 400 N	8 15 NS
PPOPAGATION DELAY TIME TO LOGICAL !	0.53	CL= 15 PF, RL= 4 00	40 55 NS

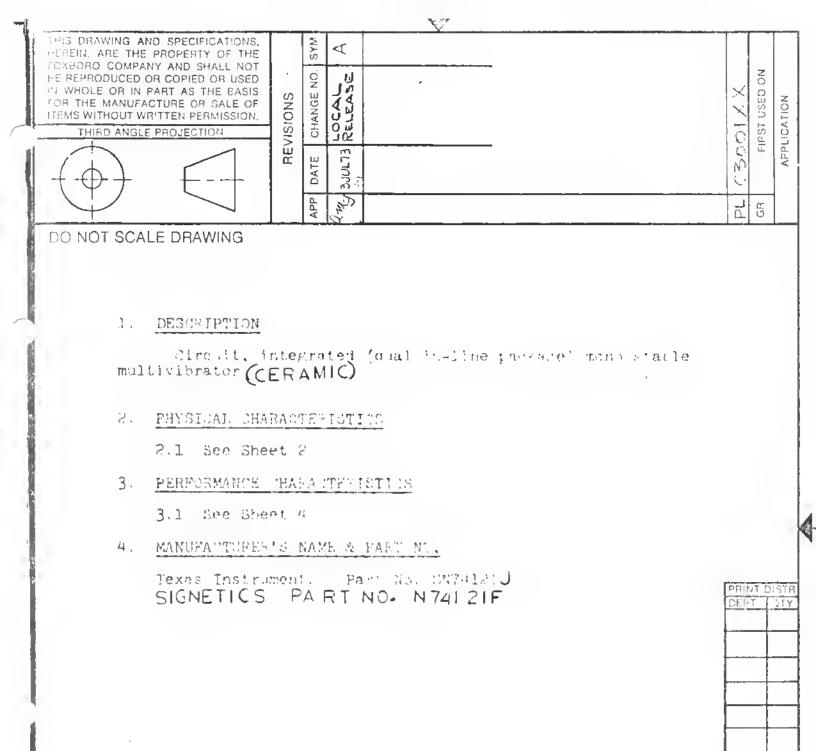
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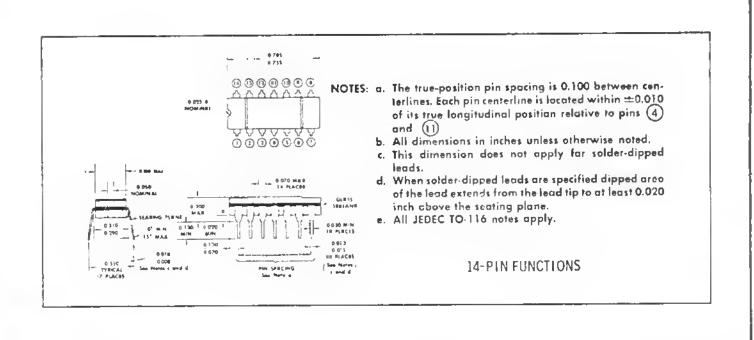
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Sheet

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THE FOXBORO COMPANY SYSTEMS DIVISION

CIRCUIT TYPES SH54121, SH74121 MONOSTABLE MULTIVIERATORS

logic

TRUTH TABLE (See Notes 1 thru 3)

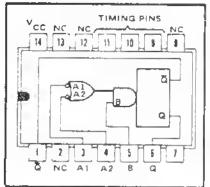
t _n	INPU	T	Ę _{n+1}	INPL	J T	OUTPUT
A1	A2	8	A1	A2	В	001701
	1	0	1	j i	7	Inhibit
0	X	1	0	Х	0	Inhibit
×	0	1	[X	0	0	Inhibit
0	×	0	0	X	1	One Shot
X	0	C	X	٥	1	One Shot
1	1	1	×	0	1	One Shot
-1	1	1	0	Х	1	One Shot
X	0	0	×	1	0	Inhibit
0	X	0	1	х	0	Inhibit
X	0	1 1	1	1	1	Inhibit
0	Х	1	1	1	1	Inhrbit
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 $1 - V_{in(1)} > 2 V$ $0 - V_{in(0)} < 0.8 V$

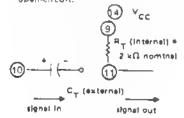
NOTES: 1. t_n = time before input trensition.

- 2. t_{n + 3} * time after input transition.
- X Indicates that either a logical 0 or 1, may be present
- 4. NC = No Internal Connection.

J OR N DUAL-IN-LINE PACKAGE {TOP VIEW} (SEE NOTES 6 THRU 9}



- A1 and A2 are negative-edge triggeredfogic induct, and will trigger the one shot when either or both go to logical 0 with 8 at logical 1.
- 8. Bits a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical t with either A1 or A2 at logical 0, ISee Truth Table1
- External timing cepacitor may be connected between pin (3) (positive) and pin (3). With no external codecitance, an output pulse width of typically 30 ns is obtained.
- B. To use the internel timing relator
 (2 k\Omega nominal), connect pin (4)
 pin (4)
- To obtain variable putse width connect external variable resistance between pin and pin No external current limiting is needed.
- 10. For accurate repeatable pulse widths connect an external resistor between pin 13 and pin 44 with pin 9 open-circuit.



SIZE SYMBOLS DRAWING NO.

A B C 3313AS A

SCALE: SHEET 3 OF 4

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V 50838 (6/67)

CIRCUIT TYPES SN54121. SN74121 MOROSTABLE MULTIVIBRATORS

electrical characteristics over operating free-air temperature range

	PARAMETER	TEST FIGURE		FIGURE TEST CONDITIONS!				UNITS
V _T , Posi	tive-going thrashold voltage at A input	57	V _{CC} - MIN			1,4	2	V
V _{T_Negs}	tive-going shieshold voltage of A input	57	V _{CC} - AHA		0.8	1 A		V
V _{T+} Poin	rea-going threshold voltage at B input	57	V _{CC} = MIN			1,55	2	V
V _{T_} Nege	live-grang thristicals votinge at 8 input	57	VCC * MIN		0.8	1.35		V
V _{ouII} 01	Logical 0 output voltage	, 57	V _{CC} + M1N, I _{MAK} + 16 mA			0.22	0.4	V
V _{0u1 1}	Logical 1 output vollage	57	VCC = MIN. I load = -400 µA		2.4	33		V
18[0]	Logical D level input current at A1 or A2	58	VCC - MAX, VIN - 0.4 V			- 1	~16	mA
inl0l	g) Logical D level input current et B 59 VCC = MAX, V _{IN} = 0.4 V		i		- 2	- 3.2	mA	
	Logical 1 level input	60	VCC - MAX. Vin - 24 V			2	40	μA
Ial1)	current at A1 or A2	00	VCC - MAX, Vin - 55 V			0.06	1	mA
	Logical 1 level input	61	VCC - MAX, VG - 74V			4	80	μE_t
rafff	current et 8		VCC - MAX, Vm - 65 V			D 05		mA
	Short execut output	67		SN54121	- 20	-25	55	
os	current et 0 or 0 f	end 63	VCC * MAX	SN74121	- 18	-75	55	mA
cc ·	Power supply current in quiescent (unlined) state	64	V _{CC} - MAX			13	25	mA
сс	Power supply current in filed state	64	VCC - MAX	1		23	40	mA

device type.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST FIGURE	TEST	CONDITIONS	MIN	TYP	MAX	UNIT
1 _{pd1}	Propagation devey time to logical 1 level from 8 input to Q output	72		C = P0 + C	15	35	55	nı
¹ pdl	Propagation defay time to logical 1 level from A.1. # 2 inputs to O output	14	CL = 15 pF.	C _T + 80 pF	25	45	70	796
1 _{pd} 0	Propagation deley time to logical Di level from 8 inout to Q output	72			20	40	65	ms
¹ pd0	Propagation (serey time to logical Dilever from A 1/A2 inputs to Q output	12	C _L = 15 pF.	C _F - 90 pF	30	50	80	nı
Iplovil	Pulse width obtained using internal filming resultor	73	CL = 15 pF. RT = Open,	CT = 80 pF.	70	110	150	ni
Palouti	Pulse width coteined with zero timing capacitation	73	CL = 15 pF. Ry = Open.	C _T = 0, Pin (9) 1d V _{CC}	20	30	50	P B
1	Puter width obtained using	73	CL = 15 pF. By = 10 kΩ,	CT + 100 pF. Pin (2) Com	600	700	800	ri is
1plous)	external timing retistor	/3	CL = 15 oF. AT = 10 kf1,	CT = 1 uF Pin @ Open	6	7	0	Ins
Thold	Minimum dunition of trigger pulm	73	CL = 15 pF. By = Open,	CT - 80 LF. Pin (9) 10 VCC		30	50	l'té

Ì	SIZE	SYMBOL DRAWING NO.			REV
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	SCAL	Ε:	SHEET 4	OF	4

^{\$}All typical values are at V_{CC} = 6 V, T_A = 25 °C. § Not more than one output should be shorted at a time,

H	. KEVISIONS		·	
10.3	DESCRIPTION	CODE	DATE	REVIEW DV
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"LEV STATUS	REV	I.A.	17.	$+\Lambda$													
OF SHEETS	SHEFT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
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	0.561.85 F 1/1.75 .					2	THEE INTEGRATED CIPCUIT USY439H TAD-SINEUT WAND DUFFER GATE-OPEN COLUMNICE OFFICE								wywa i d		
FRITOINS TOTERCHANGEAPLE TOTERCHANGEAPLE	YES .	MERCYLO		11.			SIZE						JAN 3			brH	ARRES BARRA
THEO FCO	3		F			i	SCALI	E			14	1	SH	FET	(0F [elligie pani. A

1.0 DESCRIPTION Integrated Circuit US7439H

Quad-2-Input NAND Buffer Cate-Open Collector Output

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14-Pin Hermetically Sealed. See fig # 1

3.0 PERFORMANCE CHARACTERISTICS

Diode Clemping on all Inputs
Low Power Dissipation
High Noise Margin: 1 Volt
Supply Voltage Vcc: 5 Volts ± 5%
Operating Temp. Range: 0°C to + 70°C

4.0 QUALITY ASSURANCE PROVISIONS
Inspect per this drawing

5.0 MANUFACTURER'S NAME AND PART HUMBER

SPRAGE, Electric Company North Adams, Mess P/W # US7439H

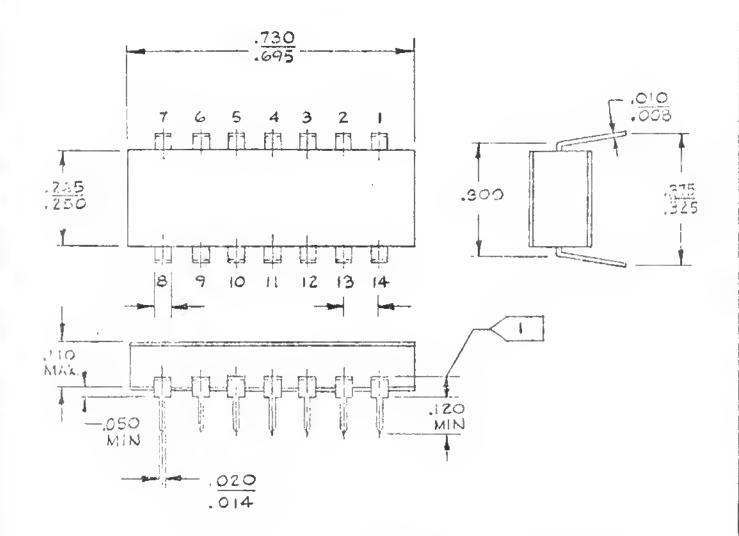
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NOTES:

- LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE,
 - 2. LEAD SPACING TOLERANCE IS NON CUMULATIVE.

FIGURE I

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	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 1912			

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OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
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DESIGNED FOR		CORPORAT RELEASE			\rightarrow	_	SCALI	Ε			٧	/T	SH	IEET	1 (OF <u>5</u>	
FORM 5758-C (5/69)	-						4										

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package) Quadruple 2-Input Positive Nand Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

4. MANUFACTURER'S NAME AND PART NUMBER

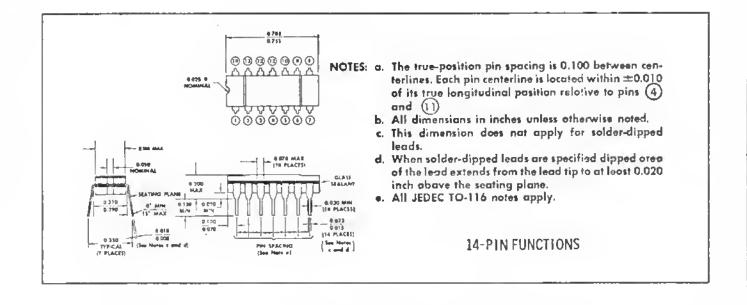
Texas Instrument, Part No. SN7400N Sprague Part No. USN7400A National Semi-conductor Corp. Part No. DM8000N Motorola Part No. MC7400P

NOTE: Only the item described on this drawing when procurred from the mfg. listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

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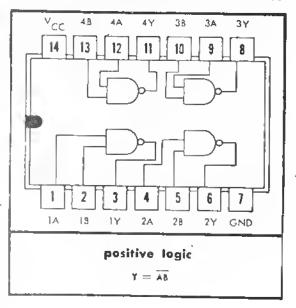
THE FOXBORO COMPANY SYSTEMS DIVISION

B V3008EA

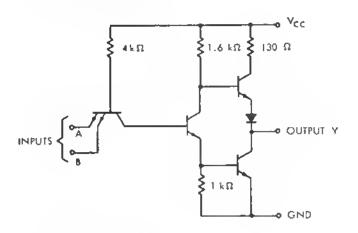
Sheet 3 of

Rev.

SN7400N
QUADRUPLE 2-INPUT POSITIVE NAND GATE



schematic (each gate)



Component values shown are combinet.

THE FOXBORO COMPANY B V =

Rev.

Sheet 4 of

recommended operating conditions

electrical characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$

	PARAMETER	TEST FIGURE	TEST CO	NOITIONS	MIN	TYP	MAX	UNIT
V _{in(1)}	Lagical 1 input valtage sequised at all input terminals to ensure lagical 0 level at autput	1	V _{CC} = 4.75 V,	$V_{out 0 } \leq 0.4 V$	2			٧
Vintel	Lagical 0 input valtage required at any input terminal to ensure lagical 1 level at output	2	V _{CC} = 475 V,	$V_{out[1]} \ge 2.4 V$			0.8	٧
V _{out[1]}	Logical 1 autput valtage	2	$V_{CC} \approx 4.75 V,$ $I_{totd} = -400 \mu A$	V _{in} = 0.8 V _i	2.4	3.3‡		٧
٧ مياڙه	Logical O output voltage	1	$V_{GC} = 4.75 V_c$ $I_{sink} = 16 \text{ mA}$	V _{in} = 2 V.		0.22‡	0.4	٧
1,0[0]	Lagical O level input current (each input)	3	V _{CC} ≈ 5.25 V,	V _{sn} = 0.4 V			∽1.6	mA
	Lagical 1 level input current (each Input)	4	$V_{CC} = 5.25 \text{V},$	V ₁₀ = 2.4 V			40	μА
lo(t)	togical i level input turrent (each input)	1 1	V _{CC} = 5.25 V,	V _{in} = 5.5 ∨			1	mA
los	Short-circuit output current†	5	V _{CC} = 5.75 V,		- 16		-55	mA
Iccio)	Legical O level supply current (each gate)	6	V _{CC} = 5 V ₁	V _{in} = 5 V		3‡		mA
Iccin	Logical 1 level supply current (each gate)	6	V _{CC} = 5 V,	V ₁₀ = 0		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 10

FARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
† _{pda} Propagation delay time to logical O level	50	C ₁ = 15 pF		8	1.5	40
t _{pd1} Propagation delay time to lagical 1 level	50	C ₁ = 15 pF		18	29	nı

†Not more than one output should be shorted at a time,

\$These typical values are of $\rm Y_{CC} = 5$ V, $\rm I_A = 25^{\circ} C_{\star}$

THE FOXBORO COMPANY SYSTEMS DIVISION

B V3008 EA

Sheet 5 of 5

= 5039 (6/68)

1				
	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	Local Release ECN 1912			

REV STATUS	REV	A	Α	Α	Α	A	A	Α									
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
UNLESS OTHERWISE																	
TITLE Circuit, Integrated Dual In-Line Package Type SN7401N																	
SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO																
DESIGNED FOR		CORPORA RELEASE						E			W			EET	1 '	OF	7

FORM 5758-C (5/69)

1.0 DESCRIPTION:

Circuit, Integrated (Dual In-Line Package) Quad 2-Input Nano Gate W/Open Collector Output

- 2.0 PHYSICAL CHARACTERISTICS:
 - 2.1 See Sheet 3.
- 3.0 PERFORMANCE CHARACTERISTICS:
 - 3.1 See Sheets 5, 6, & 7.
- 4.0 QUALITY ASSURANCE PROVISIONS:

Inspect per this drawing.

Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without engineering approval.

5.0 VENDOR'S NAME AND PART NO .:

Texas Instrument, Part No. SN7401N Sprague Part No. USN7401A Motorola Part No. MC7401P

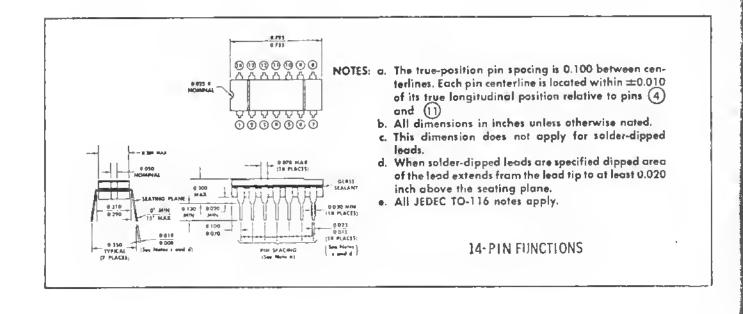
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A B V3008EB REV

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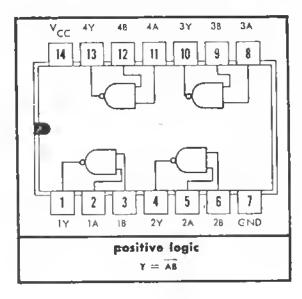


THE FOXBORO COMPANY SYSTEMS DIVISION

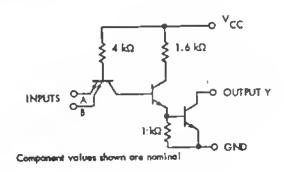
B V3008 EB

Sheet 3 of

SN7401N
QUADRUPLE 2-INPUT POSITIVE NAND GATE (WITH OPEN-COLLECTOR OUTPUT)



schematic (each gate)



THE FOXBORO COMPANY BV3008EB

Shoot Ground of

APPLICATION DATA

combined for-out and wire-OR copabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with othes similar TTL gates to perform the wire-OR function, and simultaneously, will drive from one to nine TTL loads. When no other open-collector gates are paralleled, this gate may be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and I_{aff} current (through paralleled outputs) will be available during a logical 1 level at the autput. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output volrage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_{\underline{k}} = \frac{V_{\underline{k}\underline{k}}}{I_{\underline{k}\underline{k}}}$$

where: V_{RL} is the voltage drop in volts, and I_{RL} is the current in emperes.

logical 1 (off level) circuit calculations (see figure E1)

The allowable voltage drop across the load sesistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level sequired at the loads

$$V_{RL} = V_{CC} - V_{aut(1)}$$
 required

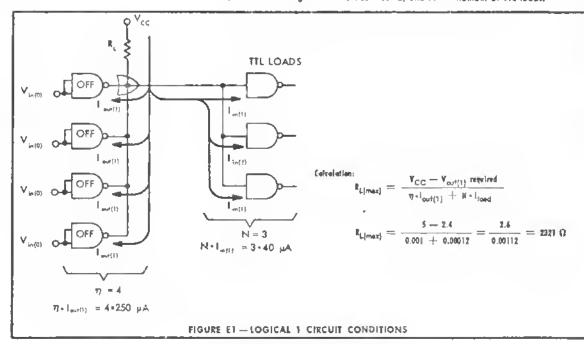
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IR(1)}) and off-level severse currents (I_{IR(1)}) through each of the wire-OR connected outputs:

$$\mathbf{I}_{\mathrm{RL}} = \mathbf{y} \cdot \mathbf{I}_{\mathrm{out}[1]} + \mathbf{N} \cdot \mathbf{I}_{\mathrm{in}[1]}$$
 to TTL loads

Therefore, calculations for the moximum value of $R_{\rm L}$ would be:

$$R_{L[max]} = \frac{V_{CC} - V_{out(1)} \text{ required}}{\pi \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: $\eta = \text{number of gates wire-OR connected, and N} = \text{number of TIL loads.}$



THE FOXBORO COMPANY SYSTEMS DIVISION

B V 3008 EB

Sheet 5 of

APPLICATION DATA

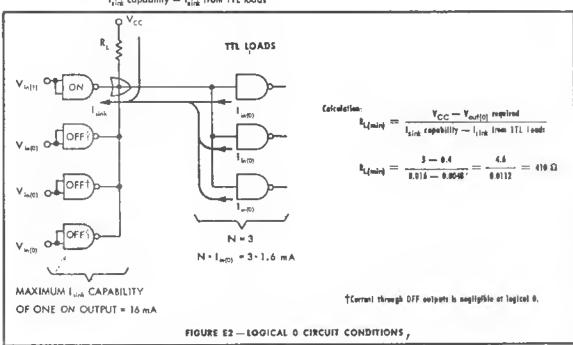
logical O (on level) circuit colculations (see figure E2)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-OR connected, the current through $R_{\rm L}$ may be shared by those paralleled transistors. However, unless it can be obsolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 16 mA, the maximum current which will essure a logical 0 maximum of 0.4 volts.

Also, for-our must be considered. Part of the 16 mA will be supplied from the Inputs which are being driven. This reduces the amount of current which can be allowed through $R_{\rm c}$.

Therefore, the equation used to determine the minimum value of $R_{\rm c}$ would be:

$$. \ R_{L[min]} = \frac{V_{CC} - V_{out(0)} \ required}{I_{Link} \ capability - I_{Link} \ from \ TTL \ loads}$$



driving T7L loads and combining autputs

Table 1 provides minimum and maximum resistor values, colculated from equations shown above, far driving one to ten TTL loads and wire-OR cannecting two to seven parallel autputs. Each value shown for wire-OR autput are it determined by the fan-out plus the leakage of a single output transistor. Extension beyond seven wire-OR connections is permitted with fan-outs of seven at less if a valid minimum and maximum $R_{\rm L}$ is possible. When fanning-out to ten TTL loads the calculation for the minimum value of $R_{\rm L}$ indicates that an infinite resistance should be used ($V_{\rm RL} \div 0 \equiv \infty$;) however, the use of a 4-kΩ resistor in this case will satisfy the logical 1 condition and limit the logical 0 level to less than 0.43 V.

TABLE 1

FAM-OUT	Ţ~		16	TRE-DR	OUTPU	15		
TO TTE LOADS	1	2	3	4	5	- å	7	1 to 7
ì	2945	4814	3291	2500	2015	1688	1452	317
Z	2828	4172	3132	2407	1954	1645	1470	2)7
3	7:27	4173	21.17	2321	1577	1604	1373	413
- 4	230	3:39	25.17	27.43	1543	1566	1361	479
5	3777	3714	1355	2166	17/3	1529	1333	175
*	3, 16	5513	2514	1098	1744	1494	13.15	718
7	4275	3333	2514	2031	1699	1460	1783	9/8
ı	4381	3170	24:7	1949	1654	X	Х	1-37
+	47.12	5023	X	X	X	X	X.	:::5
10	4069	X	I,	X	Х	Х	X	2 MB
			М	AXIMUN				RIN
			LOAD R	E515101	YALUE	IN OR	MS	

X --- Not recommended oc nal possible.

1 - The theoretical value is at . See explanation in text.

All values shown in the table are based on:

Logical II conditions: $Y_{CC}=5$ Y, $Y_{cul|11}$ required = 2.4 Y Logical II conditions: $Y_{CC}=5$ Y, $Y_{cul|01}$ required = 6.4 Y

THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 6 of

Ray.

recommended aperating conditions

Supply Voltage V _{CC}														43	/5 Y	to 5.2	5 Y
Fon-Out From Each Output, N																1 to	10

electrical characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C^{+}$

	PARAMETER	TEST FIGURE	TEST CO	NDITIONS	38.554	TYP	MAX	UNIT
Vegi	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V _{CC} = 475 V _s	$V_{\rm ext(0)} \leq 0.4 \rm V$	2			٧
V _{in(e)}	Logical O Input valtage required at any input terminal to ensure logical 1 level at output	2	Y _{CC} = 475 Y ₁	V _{euf(1)} ≥ 2.4 V			0.8	٧
V _{eut[t]}	Legical 1 output voltage	2	$V_{CC} = 4.75 \text{ V,}$ $I_{load} = -400 \mu\text{A}$	V _{in} = 0.8 V.	2.4	3,3‡		٧
V _{eur(0)}	Logical O autput valtage	1	$V_{CC} = 4.75 \text{ V},$ $I_{sink} = 16 \text{ mA}$	V _{in} = 2 V.		0.22‡	0.4	v
$I_{in(0)}$	logical O level input current (each Input)	3	$V_{CC} = 5.25 V_{\bullet}$	V _{in} = 0.4 V			-1.6	mA
(_{io(1)}	Lagical 1 level (nput current (each Input)	4	V _{CC} = 5.25 V _s	$V_{ie} = 2.4 \text{ V}$			40	μA
Juli		•	V _{CC} ≈ 5.25 V _s	V _{ie} = 5.5 V			1	mA
los	Shart-circuit output current†	5	V _{CC} = 5.25 V ₁		- 18		-55	mA
logiaj	Logical O level supply current (each gate)	6	V _{CC} = 5 V _s	V _{in} = 5 V	-	3‡		mA
$I_{CC[t]}$	Lagical 1 level supply current (each gate)	6	V _{CC} = 5 V _s	$V_{in} = 0$		1.2		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25 \, ^{\circ} C$, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	זואט
†pdo Propagation delay time to logical O level	50	C ₁ = 15 pF			15	0.1
† _{pd1} Propagation delay time to logical 1 level	50	C ₁ = 15 pF		18	29	ns.

Not more than one autput should be shorted at a time,

\$These hypical values are at $\rm Y_{CC}=5~Y_{\star}\,T_{A}=25^{o}C$

THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 7 of 7

				REVISIONS			
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SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	APPROVED LOCAL RELEASE			1.0	124/21											
DESIGNED FOR		CORPORAT RELEASE			\rightarrow	118 8	SCALI	E			W	/Т	SH	EET	1 (OF Z	- [

FORM 5758-C (5/69)

Circuit, Integrated Quad 2-Input Nor Gate

PHYSICAL CHARACTERISTICS

14 Pin Dual in-line package For more detailed physical characteristics see mfg.'s catalog.

PERFORMANCE CHARACTERISTICS

Supply Voltage Vcc: 4.75V to 5.25V

Fan Out: 1 to 10

Ambient Temperature: 0°C to 70°C

For more detailed performance characteristics see mfg.'s catalog,

QUALITY ASSURANCE PROVISIONS

Inspect per parameters outlined in mfg.'s catalog.

MANUFACTURER'S NAME AND PART NUMBER

Texas Instrument: SN7402N

Sprague: USN7402A Motorola: MC7402P

NOTE: Only the item described on this drawing when procurred from

the manufacturers listed hereon for use. A substitute item

shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

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SCALE: SHEET 2 OF 2

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ı		REVISIONS			
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		DESIGNEO	_							JAL	711 111 126	1/1/-	TEG JE 1	DAC			
SUPERSEOING INTERCHANGEABLE SIMILAR TO	YES NO	LOCAL RELEASE				1/4	SIZE		B	>		\bigvee	DRAV 30	VING DC	NUM S	BER EE	
OESIGNED FOR		CORPORA RELEASE		Edest		13,52	SCALE				W	Т	SH	EET	ì (OF 🖆	
FORM \$750 C (5/40)	_						A										

Circuit, Integrated (Dual In-Line Package)
Triple 3-Input Positive Nand Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

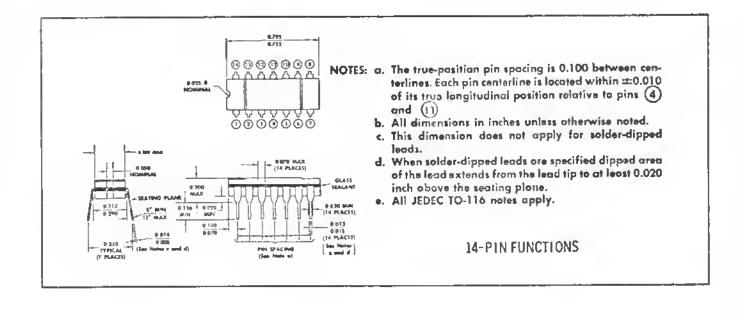
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7410N Sprague Part No. USN7410A National Semi-conductor Corp. Part No. DM8010N Motorola Part No. MC7410P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING ND.

A SCALE: SHEET DF



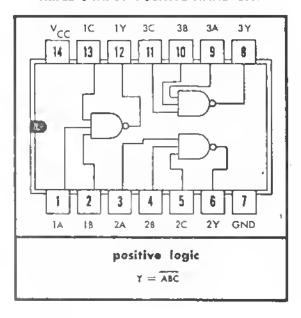
THE FOXBORO COMPANY SYSTEMS DIVISION

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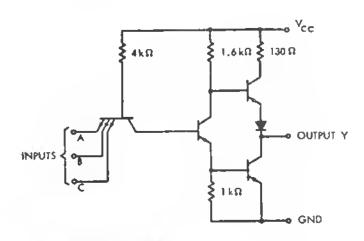
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Sheet 5 of

SN7410N
TRIPLE 3-INPUT POSITIVE NAND GATE



schematic (each gate)



Companies unless shown are naminal.

THE FOXBORO COMPANY SYSTEMS OLVISION

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recommended aperating canditions

electrical characteristics, $T_A = 0$ °C to 70°C

	PARAMETER	TEST FIGURE	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
V _{in() [}	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V _{CC} = 4.75 V,	V _{eu1 0}} ≤ 0.4 V	2		- III-OA	٧
V _{in(0)}	Lagical D input voltage required at any input terminal to ensure lagical 1 level at autput	2	V _{CC} = 4.75 V,	$V_{out[1]} \ge 2.4 V$			0.0	v
V _{out[1]}	Logical 1 autput voltage	2	$V_{CC} = 4.75 \text{ V},$ $I_{tood} = -400 \mu\text{A}$	V _{in} = 0.8 V _s	2.4	3.3‡		٧
Y _{out[0]}	Logical O autput voltage	1	$V_{CC} = 4.75 V_s$ $I_{tink} = 16 \text{ mA}$	V _{in} = 2 V.		0.22‡	0.4	٧
I ₄₀ (0)	Logical D level input current (each input)	3	V _{CC} == 5.25 V _s	V = 0.4 V			~1.6	mÁ
l _{iri(1)}	Logical 1 level input current (each input)	4	$V_{CC} = 5.25 \text{ V},$ $V_{CC} = 5.25 \text{ V},$	V _{in} = 2.4 V V _{in} = 5.5 V			40	μA mA
los	Short-circuit autput current†	5	V _{CC} = 5.25 V	10 010 7	18		-55	mA.
Iccial	Lagical O level supply current (each gate)	6	V _{CC} = 5 V.	V _{.n} = 5 V	- 10	3 ‡	-33	mÁ
(gcn)	Lagical I level supply current (each gate)	6	V _{CC} = 5 V,	Y ₁₀ == 0	_	1#		mÁ

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^{\circ}\text{C}$, N = 10

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Propagation delay time to logical O level	50	C ₁ ≈ 15 pF		1	15	DE
l	t _{pd1} Propagation delay time to logical 1 level	50	$C_{\dagger} = 15 pF$		18	29	ris

Thei more than one sulput should he sherted at a time.

 $\ddagger These typical values are at <math display="inline">Y_{\rm CC}=5$ Y, $T_{\rm A}=25^{\rm o}C$,

THE FOXBORO COMPANY B V 3008 EE

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OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
TOLERANCE UNLESS OTHERWISE DECIMAL DIMENSION ANGLES	SPECIFIED	DRAWN P. WALL DRAFTING	111 -	HK'D , VIA! ;	::- 3/	DATE (1)	H)X[BOE	10	FOXE	THE BORO,	_		-	PANY TS, U	I.S.A.
		DESIGNED						(SIR		17	TITLE INT -LIK °E S	LE C	PACI	<ag< td=""><td>Du</td><td></td></ag<>	Du	
SUPERSEDING INTERCHANGEABLE SIMILAR TD	YES YES	APPROVE				24 h (m/	SIZE			Š				_	S E		
DESIGNED FOR		CORPORA RELEASE				75 m	SCALE			, , , , ,	V	/Т	SH	IEET	1 (OF 5	
FDRM 5758-C (5/69)							4										

Circuit, Integrated (Dual In-Line Package)
Dual 4-Input Positive Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

4. MANUFACTURER'S NAME AND PART NO.

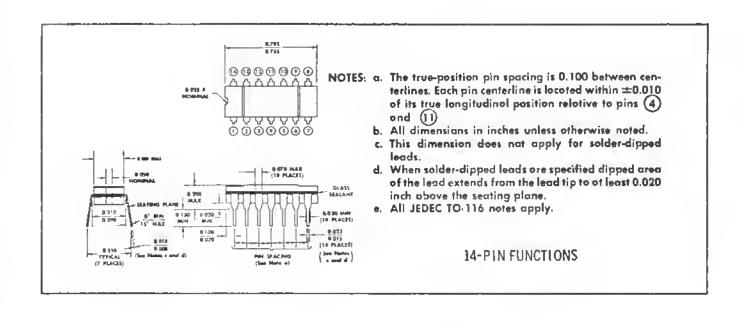
Texas Instrument, Part No. SN7420N Sprague Part No. USN7420A National Semi-conductor Corporation DM8020N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use, A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

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THE FOXBORO COMPANY SYSTEMS DIVISION

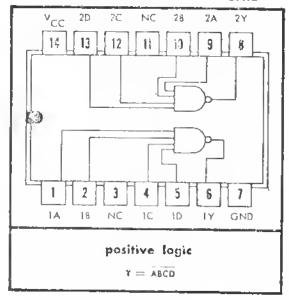
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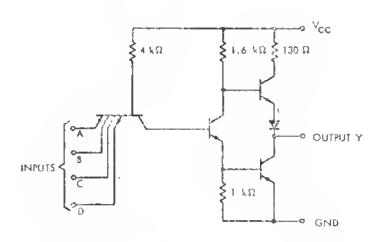
Ą

\$N7420N DUAL 4-INPUT POSITIVE NAND GATE



NC — No Internal connection, †Patented by Texas Instruments

schonatic (each gate)



Companient values shown are nominal.

THE FOXEORO COMPANY | BIVDOOGEF
SYSTEMS DIVISION | BIVDOOGEF

recommended operating conditions

electrical characteristics, $T_A == 0^{\circ}C$ to $70^{\circ}C$

	PARAMETER	TEST FIGURE	TEST CO	NDITIONS	MIN	TYP	MAX	UNIT
V _{in(1)}	Logical 1 input voltage required at all input terminals to ensure lagical 0 level at output	1	$V_{CC} = 4.75 \text{V},$	V _{ou1(0)} ≤ 0.4 V	2			٧
V _{In(0)}	Logical O input voltage required at any Input terminal ta ensure logical 3 level at output	2	$V_{CC} = 4.75 V_r$	V _{out(1)} ≥ 2.4 V			0.0	٧
V _{eut(1)}	Lagical 1 output voltage	2	$V_{CC} = 4.75 \text{ V,}$ $I_{load} = -400 \mu\text{A}$	$V_{in} = 0.8 V_{\bullet}$	2.4	\$. 5 ‡		٧
V _{out(e)}	Logical O output voltage	1	$V_{CC} = 4.75 \text{ V},$ $I_{\text{sink}} \approx 16 \text{ mA}$	$V_{in} = 2 V_{i}$		0.22‡	0.4	٧
I _{In(0)}	Lagical O level Input current (each Input)	3	V _{CC} = 5.25 V.	V _{in} = 0.4 V			-1.6	mA
		2	$V_{CC} = 5.25 V_{r}$	V _{in} = 2.4 V			40	μA
l _{in(1)}	Lagical 1 level in:put current (each Ingul)	*	$V_{CC} = 5.25 V.$	V _{in} = 5.5 V			- 1	mA
los	Shart-citcult autput current	5	V _{CC} = 5.25 V		-18		-55	mA
J _{CCRI}	Lagical O level supply current (each gate)	6	V _{CC} = 5 V,	V _{in} = 5 V		3‡		mA
	Logical 1 level supply current (each gate)	6	V _{CC} = 5 V.	V _{In} == 0		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNII
t _{pd0} Propagation delay time to logical O level	50	C ₁ = 15 pF		8	15	ns.
t _{pd1} Propagation delay time to logical 1 level	50	C ₁ = 15 pF		18	29	ns.

†Not more than one output should be sharted at a time, ‡1bose typical values are at $Y_{\rm CC}=5~Y_{\rm s}~I_{\rm A}=25^{\rm o}{\rm G}$

THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 5 of 5

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	REVISIONS			
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
$A \perp$	LOCAL RELEASE PER ECH NO. 1912.			

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-	REV STATUS	REV	A	A	A	<u>A</u>	A											
	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
-\-	TOLERANCE UNLESS OTHERWISE DECIMAL DIMENSION ANGLES	SPECIFIED	DRAWN DRAFTING DESIGNED		1K'0 . W.////	(r). (1)	ATE 23	demonstration.		CIR	CUI	T, 1	TITLE	MAS EGF	SACH SATI	ED GE	TS, U	J. S. A.
ı	SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	APPROVED LOCAL RELEASE	_			1/2	SIZE		T	Ś		V:	DRAY 3C	VING	MUM E	BER E	·
	DESIGNED FOR		CORPORA RELEASE				12-12	SCALI	E			٧	/Т	SH	EET	1 (OF 5	
	FDRM 5758-C (5/69)							4										

Circuit, Integrated (Dual In-Line Package) 8-Input Positive Nand Gate

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 3.
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 5.
- 4. MANUFACTURER'S ANME AND PART NO.

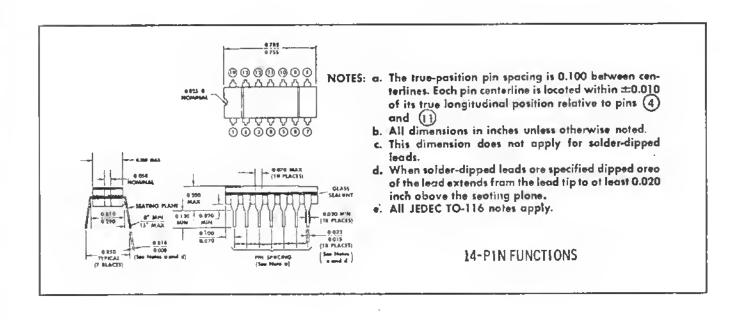
Texas Instrument, Part No. SN7430N Sprague Part No. USN7430A Motorola Part No. MC7430P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOLI DRAWING NO.

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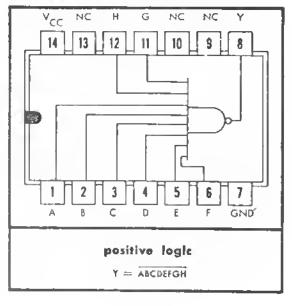
THE FOXBORO COMPANY SYSTEMS DIVISION

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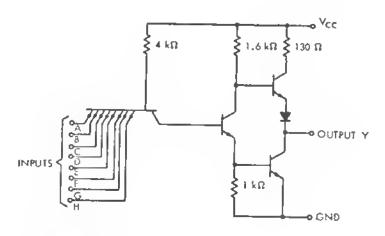
Rev.

Sheet 3 of

\$N7430N 8-INPUT POSITIVE NAND GATE



schematic



Component volves shown are nominal.

recommended operating conditions

electrical characteristics, TA = 0°C to 70°C

	PARAMETER	TEST FIGURE	TEST CON	IDITIONS	MIN	TYP	MAX	UNIT
V _{in(1)}	Logical 1 input voltage required at all input terminals to ensure lagical 0 level at autput	1	$V_{CC} = 4.75 V_c$	$V_{out 0\rangle} \leq 0.4 V$	2			٧
V _{in(0)}	Lagical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V _{CC} = 4.75 V,	$V_{\rm euf[1]} \geq 2.4~\rm V$		_	0.8	٧
V _{oul(1)}	Legical 1 autput valtage	2	$V_{CC} = 4.75 \text{ V},$ $I_{load} = -400 \mu \text{A}$	V _{in} = 0.8 V.	2.4	3.3‡		٧
V _{out[0]}	Legical O output valiage	1	$V_{CC} = 4.75 \text{ V},$ $I_{girk} \approx 16 \text{ mA}$	$V_{in} = 2 V,$		0.22‡	0.4	٧
$I_{(m/0)}$	Logical O level input current (each Input)	3	$V_{CC} = 5.25 \text{ V},$	V ₁₈ = 0.4 V			-1.6	mA
	Logical & level input current (each input)	4	$V_{CC} = 5.25 V_{\bullet}$	V ₁₀ = 2,4 V			40	μA
410(1)	Logical I level input corrent (each input)	"	$V_{CC} = 5.25 \text{ V},$	V _{in} = 5.5 V			1	mA
105	Shart-circuit autput current†	5	V _{CC} = 5.25 V		18		-55	mA
Iccial	Logical Q level supply current (each gate)	6	V _{CC} = 5 V _*	V _{in} = 5 V		3‡		mÁ
Icelli	Lagical I level supply current (each gate)	6	V _{CC} = 5 V,	V _{in} = 0		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{pd2} Prapagation delay time to logical O level	50	C _† = 15 pF		8	15	P18
t _{pd*} Propagation delay time to logical 1 level	50	C ₁ = 15 pF		18	29	- 88

†Net every than one autout should be shorted at a lime, \$\pm\$These typical values are all \$Y_{CC} = 5 Y_* T_A = 25°C.

THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 5 of 5

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	TOLERANCES UNLESS OTHERWISE S DECIMAL DIMENSION ANGLES	PECIFIED	DRAWN B W	7 .	KD N	3/2	ATE	F ()XI	30%	RO		THE BORO,					, S. A.
and the same			DESIGNED					CIRC		-		ARAT	TITLE ED E S	DL			LIN	E
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FORM 5758-C (5/69)

Circuit, Integrated (Dual In-Line Package)
Dual 4-Input Positive Nand "Power" Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4.

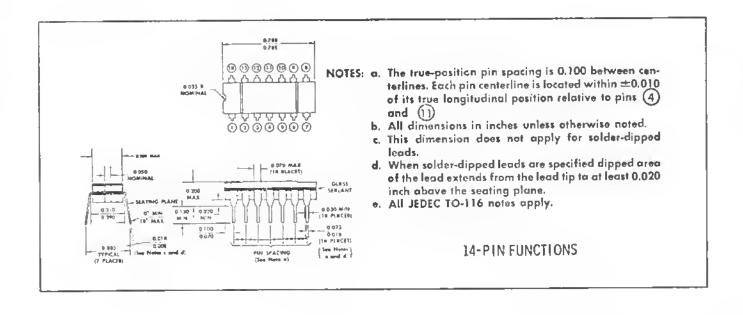
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7440N Sprague Part No. USN7440A National Semi-conductor Corp. Part No. DM8040N Motorola Part No. MC7440P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

A B [V 3008EL A SCALE: SHEET 2 OF 5



THE FOXBORO COMPANY SYSTEMS DIVISION

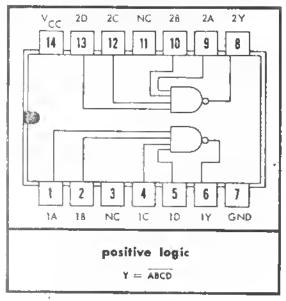
B V3008 EL

Rev.

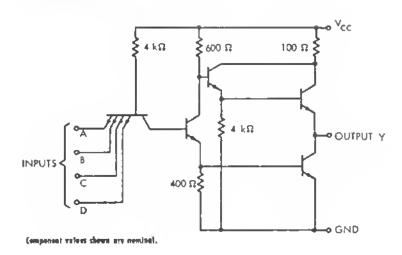
Sheet 3 of 5

Λ

SN7440N
DUAL 4-INPUT POSITIVE NAND BUFFER



schematic (each gate)



THE FOXBORO COMPANY B VBOOBEL
SYSTEMS DIVISION B VBOOBEL
Sheet 4 of 5

recommended aperating conditions

electrical characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$

	PARAMETER	TEST FIGURE	TEST COP	IDITIONS	MIN	TYP	MAX	UNIT
V _{in(1)}	Logical 1 input valtage required at all Input terminals to ensure logical 0 level at autput	1	V _{CC} = 4.75 V,	V _{ou1[0]} ≤ 0.4 V	2			٧
Y _{in[0]}	Logical D input valtage required at any input terminal ta ensure logical 1 level at output	2	$V_{CC} = 435 V$,	$V_{out[1]} \ge 2.4 \text{ V}$			0.6	٧
V _{ovf[1]}	Logical output voltage	2	$Y_{CC} = 4.75 \text{ V,}$ $I_{load} = -1.2 \text{ mA}$	V _{in} = 0.8 V,	2.4	3.3‡		٧
V ₀₀₁₍₀₎	Logical C output voltage	1	$V_{CC} = 4.75 \text{ V},$ $I_{sink} = 48 \text{ mA}$	V _{in} = 2 V,		0.28‡	0.4	٧
$I_{in(0)}$	Logical O level input current (each input)	3	$V_{CC} = 5.25 \text{ V},$	V _{an} = 0.4 V			-1.6	mA
I _{in(1)}	Logical 1 level input current (each Input)	4	$V_{CC} = 5.25 \text{ V},$	V _{or} = 2.4 V			40	μA
*****			$V_{CC} = 5.25 \text{ V},$	V _{ot} = 5.5 ∨			1	mÅ
105	Shart-circuit autput current†	5	$V_{CC} = 5.25 \text{ V}$		-18		-70	mA
ICC(0)	Logical O level supply current (each gate)	6	$V_{CC} = 5 V$	V _{in} = 5 V		8.6		mA
$I_{CC(1)}$	Lagical 1 level supply current (each gate)	6	$Y_{CC} = 5 \text{ V},$	V _{in} = 0		2 1	:	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 30

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	זואט
1pdt	Prapagation delay time to logical 0 level	50	C ₁ = 15 pF		8	15	ns
l'pd1	Prapagatian delay time to logical 1 level	50	C ₁ = 15 pF	-	18	29	ns

*Not more than one extrest should be skerted at a time.

\$These typical values are at $Y_{\rm CC}=5~V_{\rm F}T_{\rm A}=25^{6}C_{\rm c}$

THE FOXBORO COMPANY SYSTEMS DIVISION

BV300SEL

Rav.

Sheet 5 of

		REVISIONS	- ' -	2 2 2 2 2	
	LTR	DESCRIPTION	DR	DATE	APPROVED
f	Α	LOCAL RELEASE ECH NO. 1912			
	B	ECN NO. 3972	P. \$	STAUG.	BUIL

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DO NOT SCALE PRINT

1. DESCRIPTION

FIRST USED ON

Circuit, Integrated (Dual In-Line Package)
DUAL 2-WIDE 2-INPUT E/OR -INVERT GATES
VBOODEN-WITH EXPANDER INPUTS (SN7450N)
VBOODEP-NO EXPANDER INPUTS (SN7451N)

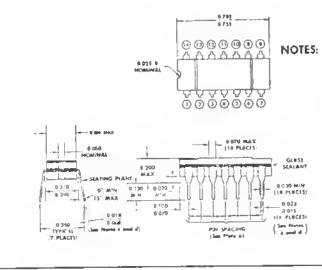
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CRARACTERISTICS
 - 3.1 See Sheet 4
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7450N/SN745IN Sprague Part No. USN7450A/USN 745IA Motorola Part No. MC7450P/MC 745IP

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

7 SH OTHERWISE SPECIFIED | WORK AUTH NO. THE FOXBORG COMPANY DIVERUSING A SHARP TOCTO FOXBORO, MASSACHUSETTS, U.S.A. DRASTONAH SENDRE NI BEA ERGISS TITLE: THEF APPLY AFTER PLATING DESIGNER CIRCUIT, INTEGRATED 150025 OH .FIONS: ± 1/64 DUAL IN-LINE PACKAGE CHECATA MALS ± .005 TYPE SN7450/SN745IN ENGINELS 3/14/2 STERIAL: SIZE SYMBOL & DRAWING NO. REV RELEASED /3008EN FEMISH: SCALE: NONE SHEET I OF LOCAL RELEASE

9053A (6/47)



NOTES: a. The true-position pin spacing is 0.100 between centorlines. Each pin conterline is located within ±0.010 of its true longitudinal position relative to pins 4 and (1)

b. All dimensions in inches unless otherwise nated.

 This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

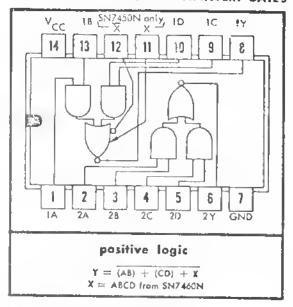
THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 EN/EP

Rov.

\$ Sheat C. of

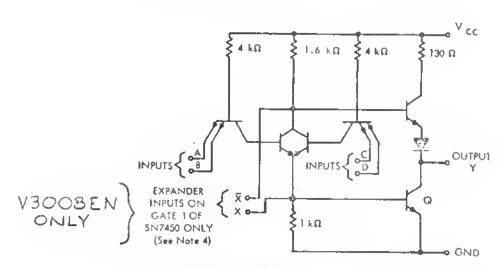
SN7450N/SN7451N DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



NOTE: Expander modes X and X are on the SX7450N acty.

Note on external connection to pins (1) and (12) of the \$X7451M.

schematic (each gate)



NOTES: 1. Compensal values shows on naminal.

2. Both SM7450 expander inputs one used simultaneously for expanding with the SM7450.

Rav.

- 3. If expander is not used focus pins 1 and 2 upon.
- 4. Make my external connection to pint 1) and 2) of the \$87451.
- 5. A lotal of four expander gates may be connected to the \$N745Q expandes.

THE FOXBORO COMPANY V3008 EN/EP

recommended operating conditions

electrical characteristics, T, = 0°C to 70°C, pins (1) and (2) apen

	PARAMETER	FIGURE	TEST CONDITIONS	мін	YYP	MAX	UNIT
V _{in(1)}	Logical 1 Input voltage required at both input terminals of either AND section to ensure lagiral 0 at output	7	$V_{\rm CC} = 4.75 V_i V_{\rm cut[0]} \leq 0.4 V$	2			٧
V _{in(0)}	tagical 0 input voltage required of and input terminal of each AND section to ensure logical 1 at output	В	V _{CC} = 4.75 V _s V _{out(1)} ≥ 2.4 V			0.8	v
V _{out[1]}	Logical 1 autput valtage	8	$V_{CC} = 4.75 \text{ V}, V_{In} = 0.8 \text{ V},$ $t_{land} = -400 \mu\text{A}$	2.4	3.3‡		٧
V _{out [0]}	Legical 0 output voltage	7	$V_{CC} = 4.75 \text{ V}, V_{in} = 2 \text{ V}, $ $I_{sink} = 16 \text{ mA}$		0.22‡	0.4	٧
In(0)	Logical O level input current (each input)	9	$V_{CC} = 5.25 V_s V_{in} = 0.4 V$			-1,6	mA
†in{I]	Logical I level Input current (each input)	10	$V_{CC} = 5.25 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{ip} = 5.5 \text{ V}$			40	μA mA
los	Short-diruit output current	11	V _{CC} = 5.25 V	- 18		-55	mA
100(0)	Logical O level supply current (each gate)	12	V _{CC} = 5 V, V _{In} = 5 V		3.7‡		mA
I _{CC[1]}	Logical 1 level supply current (each gate)	13	V _{CC} = 5 V, V _{in} = 0	-	2‡		mA

That many then one output should be shorted at a time.

Ithese hypical values are at $Y_{\rm CC}=5~Y_1~T_A=25^{\circ}C_*$

electrical characteristics (SN7450 only) using expander inputs, $T_A = 0^{\circ}C$

PARAMETER	TEST FIGUSE	TEST CONDITIONS	MIN	YYP	MAX	UMI
I _X Exponder current	14	$V_{CC} \approx 4.75 \text{ V}_1 \text{ V}_1 = 0.4 \text{ V}_2$ $I_{c-\frac{1}{2}} \approx 16 \text{ mA}$			3.1	mA
Bale-emitter voltage of output transistor (Q)	15	$V_{CC} = 475 V_1 I_{cirk} = 16 \text{ mA},$ $I_1 = 0.62 \text{ mA}, R_1 = 0$			1	٧
V _{avi(1)} Logical t output voltage	16	$V_{CC} = 4.75 \text{ V, } I_{locd} = -400 \mu A_1$ $I_{\uparrow} = 270 \mu A_2$, $I_{2} = -270 \mu A_3$	2.4	3.3‡		٧
V _{aut(0)} Logical 0 autput valtage	15	$V_{CC} = 4.75 \text{ V}_1 \text{ l}_{sink} = 16 \text{ mA}_1$ $I_1 = 0.43 \text{ mA}_1 \text{ R}_2 = 130 \Omega$		0.22‡	0.4	٧

These typical values are at $Y_{\rm CC}=5~Y_{\rm c}~I_{\rm A}=25^{\circ}C_{\rm c}$

switching characteristics, $V_{CC}=5~V,~T_A=25^{\circ}C,~pins~$ (1) and (2) apen, N=10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time to layor laginal O leval	50	C ₁ = 15 pF		8	15	nı
Francostion delay time to tpdt logical 1 layel	50	C ₁ = 15 pF		18	29	ns.

THE FOXBORO COMPANY V3006 EN/EP 800.

SYSTEMS DIVISION PARTY B

	REVISIONS			
LTR	DESCRIPTION	DR	OATE	APPROVED
Α	LOCAL RELEASE ECN NO.1912			
8_	CHG PER ECN NO. 3246	JTD	7/72	700 /2
С	ECN # 3403	12.B.	9/70	7.42

FIRST USEO ON

Circuit, Integrated (Dual In-Line Package)
Quad 2 and/or invert gate with expander inputs.
V3006ER - with expander inputs (SN7453N)
V3006ER - no expander inputs (SN7454N)

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 4
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN74 53N/SN7454N Sprague Part No. US 7453A/US 7454A Motorola Part No. MC7453P/MC7+54P

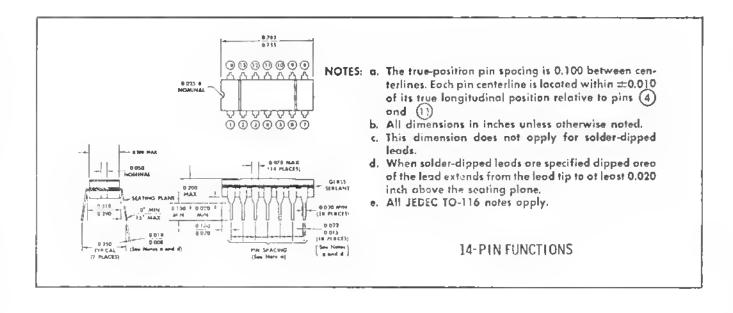
NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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ANUAS ON 210065 ± 1/64 1 1/2*		3/24/69	TITLE	DUAL I	T, INTEGRA A-LINE PAC TYPE SN745	CKAGE	
EINISH: M	RELEASED.	3/24/24	A		rawing no. √300	8ER/ES	REV C
Fr. U 60634 (6/67)	LOCAL RELEASE		SCALE:	NOME		SHEET 1 OF	-1-

4



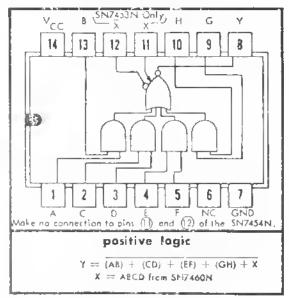
THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 ER/ES

Rev.

Sheet Z of

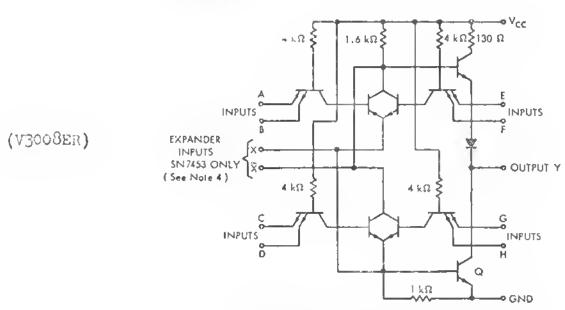
SN7453N, SN7454N 4-WIDE 2-INPUT AND-OR-INVERT GATES



KOTE - Expender codes X and X are on the SN7453H only

HC - No internal cormection. †Potential by Taxos Instruments

schematic



MOTES: 1. Component values shown are nominal,

- Both SN7453 expander inputs are used simultaneously for expanding with the SN7463.
- 3. If \$47453 expander is not used leave pins 1) and 2 spen.
- 4. Make no external connection to piles (1) and (2) of the S47454.
- A lotal of four expander gales may be connected to the SH7453 expander inputs.

THE FOXBORO COMPANY VBOOBER/ES

SYSTEMS DIVISION Shoot B of 1

electrical characteristics, $T_A = 0^{\circ}C$ to 70°C, pins (1) and (2) open

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP MAX	UNIT
V _{in(t)}	Lagical 1 input voltage required at both input terminals of either AND section to ensure lagical 0 at autput	7	$V_{CC} = 4.75 \text{ V}_{i} V_{out(0)} \leq 0.4 \text{ V}$	2		٧
V _{in{0}}	Logical C input voltage required of one input terminal of each AND section to ensure logical 1 of output	8	$V_{CC} = 4.75 \text{ V}_{aut[1]} \ge 2.4 \text{ V}_{aut[1]}$		0.8	v
V _{out(t)}	Logical 1 output voltage	8	$V_{CC} = 4.75 \text{ V}_{in} = 0.8 \text{ V}_{in}$ $I_{toad} = -400 \mu\text{A}$	2.4	3.3‡	٧
V _{out(o)}	Logical () eutput valtage	7	$V_{CC} = 4.75 \text{ V}, V_{in} = 2 \text{ V}, \\ I_{sink} = 16 \text{ mA}$		0.22‡ 0.4	٧
$I_{in(0)}$	Logical 0 level input current (each input)	9	$V_{CC} = 5.25 V_{ii} V_{iii} = 0.4 V$		-1.6	mA
I _{in(t)}	Logicol 1 level input current (each input)	10	$V_{CC} = 5.25 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{in} = 5.5 \text{ V}$		40	μA mA
los	Short-circuit output current	11	V _{CC} = 5.25 V	- 18	-55	mA
Icciol	Logical () level supply current	12	$V_{CC} = 5 \text{ V}, V_{in} = 5 \text{ V}$		3.7 ‡	mA
Icc(t)	Logical 1 level supply current	13	V _{CC} = 5 V _s V _h = 0		2 ‡	mA

†Not more than one eatput should be shorted of a flame. ‡Those typical values one at $Y_{CC} = 5 \text{ V}_{*} \text{ T}_{A} = 25 \text{ °C}_{*}$.

electrical characteristics (5N7453 only) using expander inputs, $T_A = 0$ °C

_	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	мах	UNII
l _X	Expander current	14	$V_{CC} = 4.75 V_1$ $V_1 = 0.4 V_1$ $I_{H/R} = 16 \text{ mA}$			3.1	mA
Væ[Q]	Bose-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.75 V_1$ $I_{sark} = 16 \text{ mA}$ $I_1 = 0.62 \text{ mA}_1$ $R_1 = 0$			1	٧
V ₀₀ 1[1]	Logical 1 autput voltage	16	$V_{CC} = 4.75 V_1$ $I_{load} = -400$ $I_1 = 270 \mu A_1$ $I_2 = -270 \mu$		3.3‡		٧
V _{out[0]}	Logical O output voltage	15	$V_{CC} = 4.75 \text{ V}_1$ $I_{1.0k} = 16 \text{ m/s}$ $I_1 = 0.43 \text{ mA}_1$ $R_1 = 130 \Omega$	*	0,22‡	0.4	٧

\$1hese typical values are at $Y_{\rm QQ} \, = \, 5 \; Y_{\rm H} \; 1_{\rm A} \, = \, 25^{\rm o} \xi_{\rm s}$

switching characteristics (5N7453 and 5N7454), $V_{CC}=5~V$, $T_A=25^\circ C_r$ pins (1) and (2) apen, N=10

HADAMETED		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pd0}	Propagation delay time to logical O level	50	C _t = 15 pF		8	15	P13
	Propagation delay time to lag-cal 1 level	50	C ₁ = 15 pF		18	29	ns

THE FOXBORO COMPANY VEODE ER/LC

Circuit, Integrated (Dual In-Line Package)
Dual 4-Input Expander

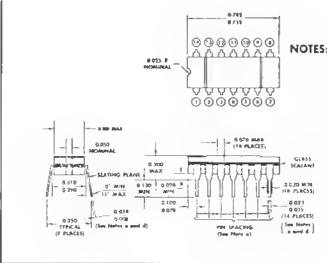
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 4
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7460N Sprague Part No. USN7460A Motorola Part No. MC7460P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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DO NOT SCALE PRINT CESS OTHERWISE SPECIFIED | WORK AUTH NO. THE FOXBORO COMPANY TVE BURG 1 & SMARP EDGES FOXBORO, MASSACHUSETTS, U.S.A. Bula BATS PERCHANTE IN INCHES JAME APOLY RETER PLATING TITLE: DESIGNES CIRCUIT, INTEGRATED NO CHOR. TiOHS ± 1/64 DUAL IN-LINE PACKAGE CHECKER WILLIAM LS ± 1/2* TYPE SN7460N Chain & 3/14/: FERIAL SIZE ISYMBOL ! DRAWING NO. REV RELEASEL V3008ET Α HallSH: SCALE: NONE LOCAL RELEASE ISHEET I OF CL : 5083A (4/87)



- NOTES: a. The true-position pin spocing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins (4)
 - b. All dimensions in inches unless otherwise noted.
 - c. This dimension does not opply for solder-dipped leads.
 - d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch obove the seating plane.
 - e. All JEDEC TO-116 notes opply.

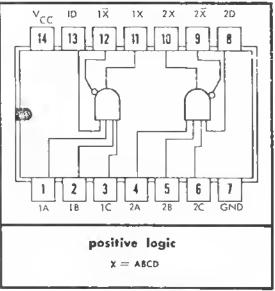
14-PIN FUNCTIONS

THE FOXBORO COMPANY SYSTEMS DIVISION

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2 Sheet of al

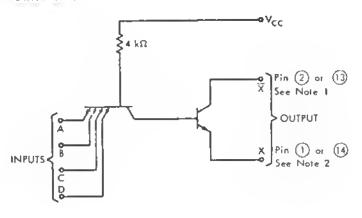
SN7460N DUAL 4-INPUT EXPANDER



NOTE: Connect pin (1) or (2) to pin (2) of SN745DN or SN745DN.

Connect pin (1) or (1) to pin (1) of SN745DN or SN745DN.

schematic



- MOTES: 1. Connect pin 2 or (13) to pin 2 of SH7450 or SH7453.
 - 2. Connect piu 1 or 14 to pin 1 uf SN7450 or SN7453.
 - 3. (amponent values shown are nominal,

THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 ET

Rev.

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recommended operating conditions

electrical characteristics (unless otherwise noted $T_A = 0^{\circ}C$ to $70^{\circ}C$)

	PARAMETER	TEST FIGURE	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
V _{in[1]}	Logical 1 input valtage required at all input terminals to ensure output on level	17	$V_{CC} = 4.75 \text{ V,}$ $R = 1.1 \text{ kH,}$		2		•	٧
V _{in(a)}	Logical O input voltage required at any input terminal to ensure output off level current	18	$V_{CC} = 4.75 \text{ V},$ $R = 1.2 \text{ k}\Omega,$ $T_A = 0^{\circ}\text{C}$	$V_1 = 4.5 \text{ V,}$ $I_{off} = 0.15 \text{ mA,}$			0.8	٧
V _{eri}	Output voltage on level	17	$V_{CC} = 4.75 \text{ V},$ $V_1 = 1 \text{ V},$ $T_A = 0^{\circ}\text{C}$	$V_{in} = 2 V_i$ $R = 1.1 k\Omega_i$			0.4	٧
l _{off}	Output off level current	18	$V_{CC} = 475 \text{ V},$ $V_1 = 4.5 \text{ V},$ $T_A = 0 ^{\circ}\text{C}$				270	μΑ
Ion	Output on level current	19	$V_{CC} = 4.75 \text{ V}, V_{t} = 1 \text{ V}$	V,n = 2 V,	-0.43			mA
i _{(n(0)}	Logical O level input current (each input)	18	V _{CC} = 5 25 V,	V _{in} = 0.4 V			-1.6	mA
I _{m(1)}	Logical 1 level input current (each input)	20	$V_{CC} = 5.25 \text{ V},$ $V_{CC} = 5.25 \text{ V},$				40	μA mA
lccled	On level supply current (each gate)	21	$V_{CC} = 5 \text{ V},$ $V_{1} = 0.85 \text{ V},$	V _{,n} = 5 V,		0.6		mA
I _{CC off}}	Off level supply current (each gate)	21	$V_{CC} = 5 V$			1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 10

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 _{pd@}	Propagation delay time to logical O level (through SN7450 or SN7453)	51	C ₁ = 15 pF		10	20	PLS.
1 _{pd1}	Propagation delay time to logical 1 level (through SN7450 or SN7453)	51	C ₁ = 15 pF		20	34	178

THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 ET

Sheet of

Rev.

	REVISIONS			
LTR	DESCRIPTION	DR	DATE	APPROVED
Α	LOCAL RELEASE ECN NO. 1912			
B	ECN # 3403	K.Fa.	-	

FIRST USED ON

Circuit, Integrated (Dual In-Line Package) Single-Phase J-K Flip-Flop

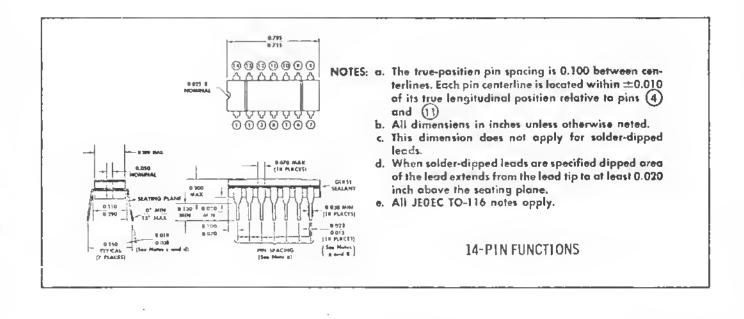
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 5
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7470N Sprague Part No. US 7470A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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LI ST OTHER SEED SEED	WORK AUTH NO.		A Company of the Comp		BORO COMPANY	
THE PLACE BEARDERS	BAATTER DOLLAR	2347	March 1981	FOXBORO, MA	SSACHUSETTS, U.S.A	ł
TEG ON	Distance			RCUIT, INTEGRAT		
16 18 ± 1/64 16 13 ± 003 17 ± 1/2°	CHECKER WY CLOW	Frake		AL IN-LIEE PACE TYPE SN7470		
STEMAL! (%	A Samuel	3/14/71	SIZE SYMBO	L BERAVING NO.	RU	atmens EV
INISH: 62	AELE#5.13		A	V300	SEW B	3
	LOCAL RELEASE		SCALE: NO		SHEET I ОР 🐧	entres.



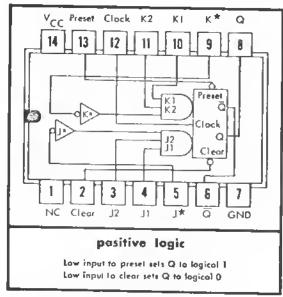
THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 EW

Rav.

Shoot 2 of 5

SN7470N J-K FLIP-FLOP



NOTE:	Clock must be at legical 0 prior to the application
	el preset er cleur functions,

TRUTH TABLE					
1	n	t_{n+1}			
)	К	Q			
0	0	Qn			
0	1	0			
	0	Ť			
1	1	Q,			

#01E5: 1. J = J1 · J2 • J k

- 2. K = K1 · K2 · K*
- 3. In = hit time bofore elock palse,
- 4. t_{n+1} == bit time alter clock gulse,
- 5. If inputs 1% or 10% ore not used.
 They must be grounded.

description

The \$N7470 is a manolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and \overline{Q} outputs. Input information is transferred to the autputs on the positive edge of the clack pulse.

Direct coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clack input threshold voltage has been passed, the gated inputs are locked out.

The SN7470 flip-flap is ideally suited far medium-and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

Supply Voltage Vcc	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Clock Pulse Transition Time to Logical 1 Level, ti(clock) (See Figure 53	3) 5 to 150 ns
Width of Clock Pulse, tplclock) (See Figure 53)	> 20 ns
Width of Preset Pulse, tp(preset) (See Figure 52)	\sim \sim \sim \sim 25 ns
Width of Clear Pulse, tp(clear) (See Figure 52)	

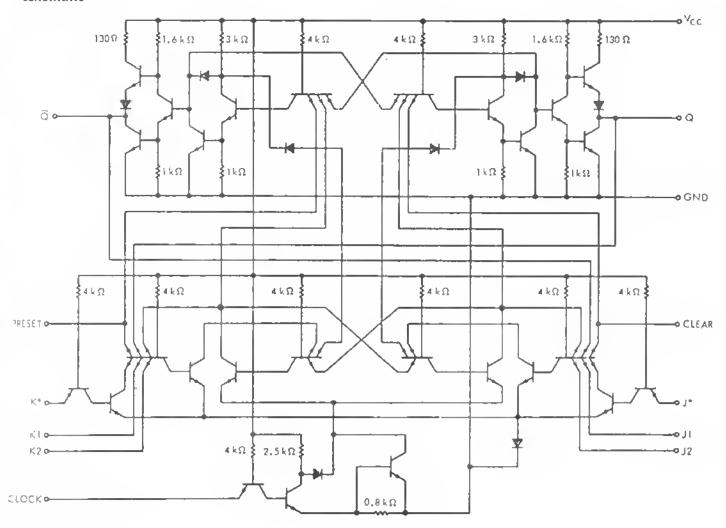
THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 EW

Rev B

Shoot 3 at 5

schematic



Companion) values shown are nominal.

THE FOXBORO COMPANY SYSTEMS DIVISION V3008EW

Shoot 4 of 5

electrical characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	บพเร
V _{rn(1)}	Input voltage required to ensure logical 1 at any input terminal	22	V _{CC} = 475 V	2			٧
V _{inf0})	Input voltage required to ensure logical () at any input terminal	23	Y _{CC} = 4.75 V			0.8	٧
$\mathbf{V}_{ou^{\dagger}\Pi 1}$	Logical 1 autout valtage	22	$V_{CC} = 4.75 \text{ V, } I_{load} = -400 \mu A$	2.4	3.5‡		v
Voutjot	logical O autput valtage	23	V _{CC} = 4.75 V, I _{sink} = 16 mA		0.22‡	0.4	V
I _{in(0)}	logical O level input current at J1, J2, J*, K1, K2, K*, az clock	24	$V_{CC} = 5.25 V, V_{in} = 0.4 V$			-1.6	mÅ
i _{in[0]}	Lagical O level input current of preset or clear	24	V _{CC} = 5.25 V, V _{III} = 0.4 V		_	-3.2	mA
l _{in[1]}	logical 1 level input current at 11, 12, 1%, K1, K2, K%, or clock	25	$V_{CC} = 5.25 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{in} = 5.5 \text{ V}$			40	μA
I _{In(1)}	Lagical 1 level input current at preset or clear	25	$V_{CC} = 5.25 \text{ V}, V_{cn} = 5.5 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{cn} = 5.5 \text{ V}$			80	μA mA
los	Shart-circuit autput current!	26	$V_{CC} = 5.25 \text{ V}, V_{v_0} = 0$	-18		-57	mÅ
loc	Supply current	25	V _{CC} = 5 V, V _{cf} = 5 V		13‡		mÅ

That more than one output should be shorted at a time,

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 10

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Eclock	Maximum clack frequency	53	C ₁ = 15 pF	20	35		Millz
t _{sa Tup}	Minimum input setup time	53	C ₁ = 15 pF		10	20	ne
t _{hold}	Minimum Input hold time	53	C, = 15 pF		0	5	ns.
ř _{pd1}	Propagation delay time to logical It lavel from clear or preset to output	52	C ₁ = 15 pF			50	ns
Îpd0	Propagation delay time to logical O level from clear or preset to autput	52	C ₁ = 15 pF			50	nı
t _{pd1}	Propagation delay time to logical I level from clock to output	53	$C_1 = 15 pF$	10	27	50	nı
Ppda	Propagation delay time to logical O level from clack to output	53	$C_{\gamma} = 15 \text{ pF}$	10	18	50	ur

THE FOXBORO COMPANY V3008 EW
SYSTEMS DIVISION Shoot F of 5

 $[\]ddagger These typical values are at <math display="inline">Y_{\rm CC}=5$ V, $T_{\rm A}=25^{\rm o}{\rm C}_{\rm c}$

	REVISIONS			
LTR	DESCRIPTION	DR	DATE	APPROVED
A	LOCAL RELEASE ETN NO. 1912			

1. DESCRIPTION

FIRST USED ON

Circuit, Integrated (Dual In-Line Package) Single Master/Slave Flip-Flop

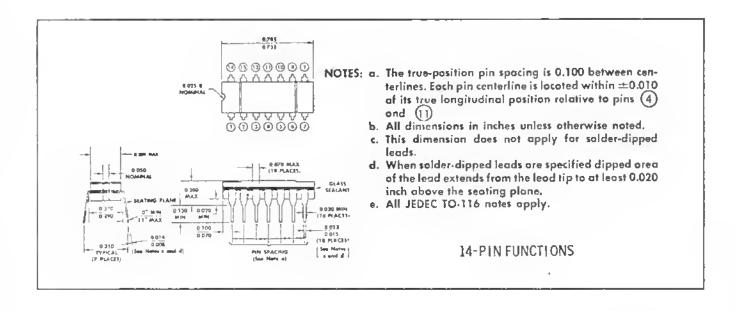
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 5
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7472N Sprague Part No. USN7472A Motorola Part No. MC7472P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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THOMS ARE IN INCHES THE FUTUR AFTER PLATING THOMS TO THE THOMS THOMS TO THE THOMS THOMS TO THE THOMS THE THE	CHE. ES	7-4/	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN74 72N	
TERIAL: A	AEL ATL	740/15	SIZE SYMBOL DHAVING NO. RE	ËV 1
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THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 EX

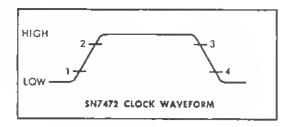
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description

The SN7472 J-K flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clack pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

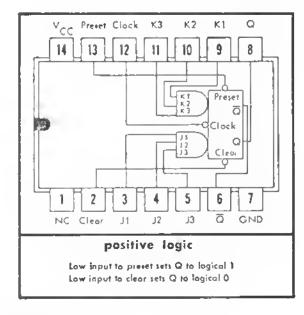
- 1. lealate slave from master
- 2. Enter information from AND gate inputs to master
- 3. Disable AND gate inputs
- 4. Transfer information from master to slave.



recommended operating conditions

Supply Valtage V _{CC}														6.75	V 1	o 5.25 V	
Fon-Out From Fach Output, N																1 to 10	
Width of Clock Pulse, tp(clock) (See Figure 54) .																≥ 20 ns	
Width of Preset Pulse, tp(preset) (See Figure 55)																≥ 25 ns	
Width of Clear Pulse, tp(clear) (See Figure 55) .																≥ 25 ns	
Input Setup Time, teetup (See Figure 54)									≥	A	eli	ad	Cle	ck	Puls	a Width	
Input Hald Time, I _{hold}																	

SN7472N J-K MASTER-SLAVE FLIP-FLOP



TRI	JTH T	ABLE
1,	1	t_{n+1}
1	K	Q
0	0	Q _n
0	1	0
1	0	1
1)	Q _n

MOLES: 1, 1 = 31 × 12 · 33
2, K = K1 × K2 × K3
3 t_n = bit time before clark pelse,
4, t_{n+1} == bit time alter clark pulse,

RC — Na internal connection. †Patented by Toxas Instruments

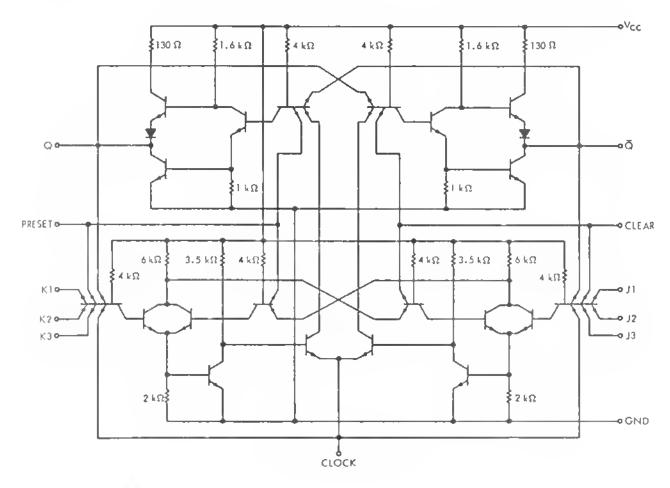
THE FOXBORO COMPANY SYSTEMS DIVISION

V 3008 EX

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Sheet - of

schematic



Component values shown ore nominal,

THE FOXBORO COMPANY V3008 EX

electrical characteristics, $T_{\rm A} = 0\,^{\rm o} C$ to $70\,^{\rm o} C$

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN TYP MAX	UNI
V _{in{1}}	Input voltage required to ensure logical L at any input terminal	27	V _{CC} = 4.75 Y	2	٧
V.n(0)	Input voltage required to enrure logical O at any input terminal	27	V _{CC} = 4.75 V	0.8	٧
V _{outtij}	Logical 1 autput voltage	27	$V_{CC} = 4.75 \text{ V}, I_{load} = -400 \mu\text{A}$	2.4 3.5‡	Ý
V _{ocit[0]}	Legical D autput voltage	28	$V_{CC} = 4.75 \text{ V}_{i}$ $I_{cirk} = 16 \text{ mA}$	0.22‡ 0.4	٧
I _{1n(0)}	Lagical O level input current at J1, J2, J3, K1, K2, or K3	29	V _{CC} = 5.25 V, V _{in} = 0.4 V	-1.6	mA
I _{in(0)}	Logical O level input current at preret, clear, or clock	29	V _{CC} = 5.25 Y, V _{in} = 0.4 Y	-3.2	mA
k _{in(1)}	Logical 1 level input corrent at £1, J2, J3, K1, K2, or K3	30	$V_{CC} = 5.25 \text{ V}, V_{IA} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{IA} = 5.5 \text{ V}$	40	μА
l _{in(1)}	Logical 1 level input current at preset, clear, or clock	30	$V_{CC} = 5.25 V_1$, $V_{ih} = 5.5 V$ $V_{CC} = 5.25 V_2$, $V_{ih} = 2.4 V$ $V_{CC} = 5.25 V_3$, $V_{ih} = 5.5 V$	80	mA μA mA
los	Short-circuit output corrent	31	$V_{CC} = 5.25 \text{ V}, V_{ID} = 0$	- 16 -57	mA
lee	Supply current	30	V _{CC} = 5 V, V _m = 5 V	8‡	mA

That mais than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 10

	PARAMETER	RAMETER TEST CONDITIONS		MIN	TYP	MAX	UNI
ficlock	Maximum clock frequency	54	$C_1 = 15 pF$	10	15		MHz
† _{pd1}	Propagation delay time to logical 1 level from clear or preset to autput	55	C ₁ == 15 pF		26	50	ns
†pd q	Propagation delay time to logical O level from clear or preset to output	55	C, = 15 pF		34	50	ns
†pd1	Propagation delay time to logical I level from clock to autput	54	C ₁ = 15 pF	10	16	50	Pal
†poq	Propagation delay time to logical O level from clock to output	54	C, = 15 pF	10	34	50	ns.

THE FOXBORO COMPANY SYSTEMS DIVISION	V300SEX	Re.
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^{\$}Their typical values are at $Y_{CC}=5\ Y_{*}\ T_{A}=25^{\circ}C.$

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FIRST USED ON		REVISIONS	_		
	LTR	DESCRIPTION	DR	DATE	APPROVED

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual Master/Slave Flip-Flop

A LOCAL RELEASE ECH NO. 1512

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 5
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7473N
Sprague Part No. USN7473A
National Semiconductor Corp. Part No. DM85D1N - Motorola Part No. MC7473P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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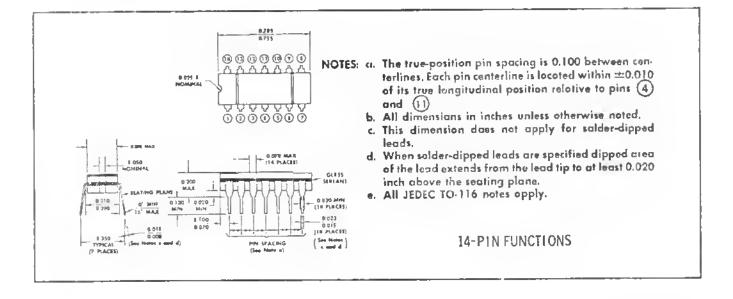
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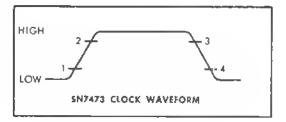


THE FOXBORO COMPANY V3008 EY

description

The SN7473 J-K flip-flop is based on the master-slave principlo. Inputs to the master section are controlled by the clock pulso. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

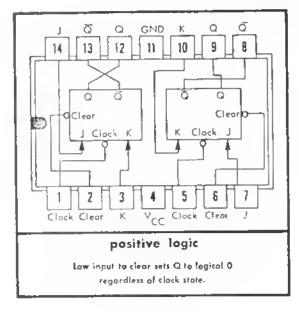
- 1. Isolate slava from master
- 2. Enter information from J and K inputs to moster
- 3. Disable J and K inputs
- 4. Transfer information from moster to slave.



recommended operating conditions

Supply Voltage V _{CC}					 						. 4.3	75 V	1o 5.25 V
Fon Out From Each Output, N													1 lo 10
Width of Clack Pulse, tp[clack] (See Figure 54) .													≥ 20 ns
Width of Clear Pulse, Policies (See Figure 55) .													
Input Setup Time, t _{setup} (See Figure 54)								≥	App	lied	Cloc	k Pi	olse Width
Input Hold Time, thold						٠							≥ o

SN7473N DUAL J-K MASTER-SLAVE FLIP-FLOP ·



TRUTH 1	TABLE (Eos	h flip-flop)
t,	1	t _{n+1}
1	K	Q
0	0	Q _n
0	1	0
1	0	1
1	1	ũ,

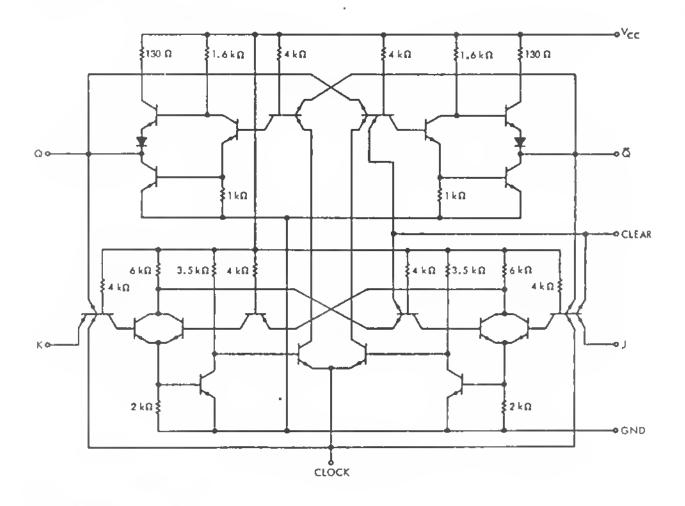
MOTES: 1, $t_n=$ bit time before cleck pulse, 2, $t_{n+1}=$ bit time after clock pulse.

THE FOXBORO COMPANY SYSTEMS OLVISION

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schematic (each flip-flop)



Compount values shown are nominal.

THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 EY

Sheet 4 m 5

electrical characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN TYP	MAX	UNIT
V _{in(I)}	Input valtage required to ensure logical 1 at any input terminal	32	V _{CC} == 4.75 V	2		٧
V _{in(0)}	Input voltage required to ensure lagical O at any input terminal	32	V _{cc} = 4.75 V		0.8	v
V _{oul[I]}	logical 1 output valtage	32	$V_{CC} = 4.75 V_i$ $I_{load} = -40$	10 μA 2.4 3.5 ‡		٧
Y _{001{0}}	Logical O sulput voltage	33	V _{CC} = 4.75 V _s I _{sirk} = 16 r	nA 0.22‡	0.4	٧
1,,,(0)	Lagical O level input current at J at K	34	$V_{CC} = 5.25 V_i \qquad V_{in} = 0.4 V_{in}$		-1.6	mA
Intol	Lagical O level input current of clear or clack	34	V _{CC} = 5.25 V _e V _{in} = 0.4 V		-3.2	mA
Liatri	Logical Hevel input current at J at K	35	$V_{CC} = 5.25 \text{ V}, \qquad V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, \qquad V_{in} = 5.5 \text{ V}$		40	μA mA
l _{in(s)}	logical i level input current atclear or clack	35	$V_{CC} = 5.25 \text{ V}_{s}$ $V_{sh} = 2.4 \text{ V}_{sh}$ $V_{CC} = 5.25 \text{ V}_{sh}$ $V_{sh} = 5.5 \text{ V}_{sh}$		80	μA mA
Ios	Short-circuit output current†	36	V _{CC} = 5.25 V, V _{in} = 0	- 18	-57	mA
1 _{CC}	Supply current (each flip-flop)	35	V _{CC} = 5 V. V ₁₀ = 5 V	8‡		mA

That more than one exigut should be skerled at a time.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25$ °C, N = 10

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fclock	Maximum clack frequency	54	C ₁ = 15 p₹	10	15		MHz
t _{pd1}	Propagation delay time to logical 1 leval from clear to output	55	C ₁ = 15 pF		26	50	ns
t _{pd9}	Propagation delay time to logical O level from clear to output	55	C ₁ = 15 pF		34	50	ms.
I _{pdI}	Propagation delay time to logical I fevel from clack to output	54	C ₁ = 15 pF	10	26	50	ns.
t _{pd0}	Propagation delay time to logical O level from clock to output	54	C ₁ = 15 pF	10	34	50	ns.

THE FOXBORO COMPANY
SYSTEMS DIVISION

Sheet 5:15

^{\$1}hese typical values are all $Y_{\rm CC}=5~Y_{\star}~1_{\rm A}=25^{\rm e}{\rm C}_{\star}$

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ANGLES ± 1" Entering and a second a second and a second and a second and a second and a second a												THE BORO,				TS, L	J. S. A .
		DESIGNED					TITLE CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7474N										
SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES	APPROVED J. P. LOCAL RELEASE				e4 (65) In / 62											
DESIGNED FOR		CORPORAT RELEASE :			_	VU 13	SCAL	E			M	/Τ	SH	EET	1 (OF 6	2

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual "D" Type Flip Flop

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 6.

4. MANUFACTURER'S NAME AND PART NO.

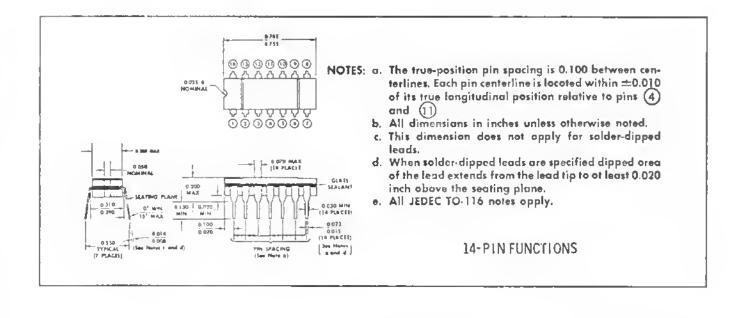
Texas Instrument, Part No. SN7474N Sprague Part No. USN7474A National Semiconductor Corp. Part No. DM8510N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL FORAWING NO.

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THE FOXBORO COMPANY SYSTEMS DIVISION

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description

The SN7474 is a monalithic, dual, D-type, edge-triggered flip-flap featuring direct clear and preset inputs and complementary Q and \overline{Q} outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

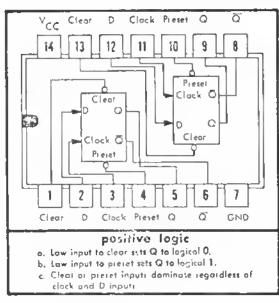
Clack triggoring occurs at a valtage level of the clack pulse and is not directly related to the transition time of the positive going pulse. After the clack input threshold voltage has been passed the data input (D) is lacked out.

The SN7474 dual flip-flop has the same clacking characteristics as the SN7470 gated (edga-triggered) flip-flop and both are ideally suited for medium, and high-speed applications. The SN7474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

Supply Valtage V _{CC}			٠.							4				4.73	5 V	to 5.25 Y
Fan-Out From Each Output, N															4	. 1 to 10
Width of Clack Pulse, tptcfack) (See Figure 56) .								4				4			4	≥ 30 ns
Width of Preset Pulse, 1 piptered (See Figure 53)														4		≥ 30 ns
Width of Clear Pulse, totalers (See Figure 53) .	4														4	≥ 30 ns

SN7474N DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



TRUTH TABLE (Each Flip-Flap)

1,,	i _n	+1
INPUT D	QUITPUT	OUTPUT Q
0	0	1
ì	1	0

MOTES: 1. t. = bit time belore clack oules.

2. in+t = bit time alter cleck pulse.

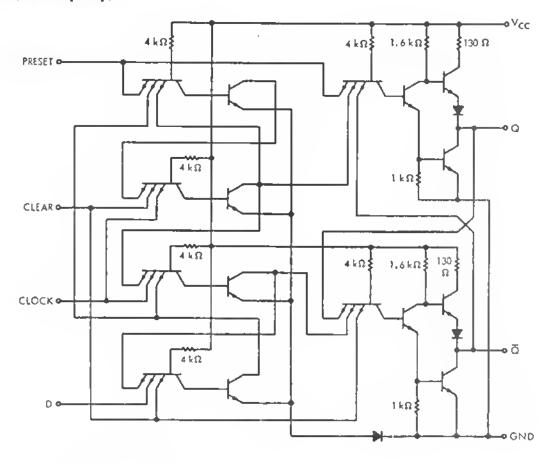
THE FOXBORO COMPANY SYSTEMS DIVISION

B 1300SEZ

Rev.

Sheet 4 of

schematic (each flip-flop)



Component values shown are nominal,

THE FOXBORO COMPANY B V3008 EZ

Sheet 5 of

electrical characteristics, $T_A = 0$ °C to 70°C

	PARAMETER	TEST FIGURE	TE	ST CONDITIONS	MIN	TYP MAX	UNI
V _{in(t)}	Input valtage required to ensure logical 1 at any input terminal	37	V _{CC} = 4.75 ∨		2		٧
V _{in[0]}	Input voltage required to ensure logical 0 at any input terminal	37	$V_{CC} = 4.75 V$			0.0	٧
$V_{out(1)}$	Logical 1 autput valtage	37	V _{CC} = 4.75 V,	$I_{load} = -400 \mu A$	2,4	35‡	٧
$V_{\infty 1[0]}$	Logical O autput vallage	38	$V_{CC} = 475 V_s$	F _{errit} == 16 mA		0.22‡ 0.4	V
I _{In(P)}	Logical O level input Current of preset of D	39	V _{CC} = 5.25 V _i	V _{in} = 0.4 V		-1,6	mA
F _{in(0)}	Logical O level input current at clear or clack	39	V _{CC} = 5.25 V ₄	V _{an} = 0,4 V		-3.2	mÅ
l _{in(1)}	Logical 1 level input	40	$V_{CC} = 5.25 \text{ V}_{c}$ $V_{CC} = 5.25 \text{ V}_{c}$	1-1		40	μA mA
I _{10[3]}	Logical 1 level input current	40	$V_{CC} = 5.25 \text{ V},$ $V_{CC} = 5.25 \text{ V},$			80	μA
I _{iol11}	Lagical 1 level input current at clear	40	$V_{CC} = 5.25 \text{ V},$ $V_{CC} = 5.25 \text{ V},$	Tr.		120	JIA.
los	Short-circuit output current	41	V _{CC} = 5.25 V.	V ₁₀ = 0	- 18	-57	_mA _mA
lcc	Supply current (each flip-flop)	40	$V_{CC} = 5 V$	V ₁₇ = 5 V		8.5 ±	mA

(these typical values are et $Y_{CC}=3~Y_{c}~I_{a}=23^{o}C_{c}$

switching characteristics, $V_{CC}\!=\!5$ V, $T_A\!=\!25^{\circ}\text{C}$, $N\!=\!10$

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNII
$f_{\rm clock}$	Maximum clack frequency	56	C ₁ = 15 pF	15	25		MHz
t _{retup}	Minimum input setup time	56	C ₁ = 15 pF		15	20	nı
I _{held}	Minimum input hold time	56	C ₁ = 15 pF		2	5	nı
f _{pd1}	Propagation delay time to logical 1 level from clear or preset to output	52	C ₁ = 15 pF			25	me
l _{pd0}	Propagation delay time to logical O level from clear or preset to output	52	C ₁ = 15 pF			40	nı
l _{pd1}	Propagation delay time to logical Lievel from clack to autput	56	C ₁ = 15 pF	10	20	35	n e
pd9	Propagation delay time to logical O level from clack to output	56	C ₁ = 15 pF	10	28	50	ns

THE FOXBORO COMPANY SYSTEMS DIVISION

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	REVISIONS			
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-	OF SHEETS	SHEET	1	2	3	4	5	ó	7	8	9	10	11	12	13	14	15	16			
	TOLERANCES UNLESS OTHERWISE DECIMAL DIMENSION ANGLES	SPECIFIED		ENVALUE - Track Francis HOXPORO										THE FOXBORO COMPANY OXBORO, MASSACHUSETTS, U.S.A							
. [1]			DESIGNED				TITLE CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7475N														
ļ	SUPERSEDING INTERCHANGEABLE SIMILAR TO	YES NO	APPROVE LOCAL RELEASE	िसा	KLES OOK		14/27 (1/29)	SIZE		B	,		DRAWING NUMBER V3008FA								
March Competition	DESIGNED FOR CORPORATE RELEASE PARACIES SAN							SCAL	E			V	T	SH	EET	\	OF \<	2			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package) Quadruple Latch

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 3.
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheets 6, 7, 8, 9, & 10.
- 4. MANUFACTURER'S NAME AND PART NO.

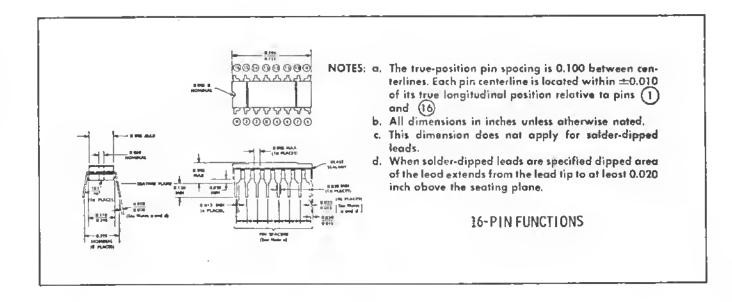
Texas Instrument, Part No. SN7475N Sprague Part No. USN7475B National Semiconductor Corp. Part No. DM8550N Motorola Part No. MC7475P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOL DRAWING NO.

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THE FOXBORO COMPANY SYSTEMS DIVISION

B V3008 FA

Rev

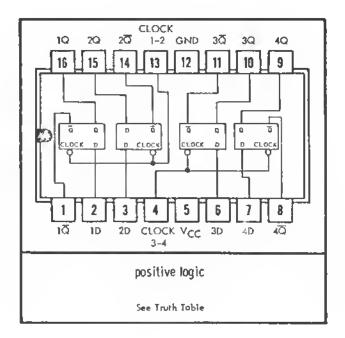
Sheet 3 of

logic

	UTH TA8 och Latel													
t _n t _{n+1}														
D	Q	۵												
1	- 1	0												
0	0	i												

NOTES:

- t = bit time before clock pulse.
- t_{n+1} = bit time ofter clock pulse.



description

The SN7475N is a monolithic, quadruple, bistable latch with complementary Q and \overline{Q} outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes law, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high. Pin assignments, or physical placement of the logical functions, were selected to coincide with the physical placement of logical functions of other Series 74 circuits which are most likely to be used as inputs to, or outputs from, the SN7475N.

This latch is ideally suited for use as temporary starage for binary information between processing units and input/output or indicator units. Applications are shown for the SN7475N being used for temporary storage of 4-bit binary data and as a dual master-slave flip-flop with two-phase clacking.

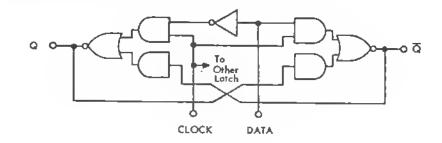
THE FOXBORO COMPANY SYSTEMS DIVISION

B V3008 FA

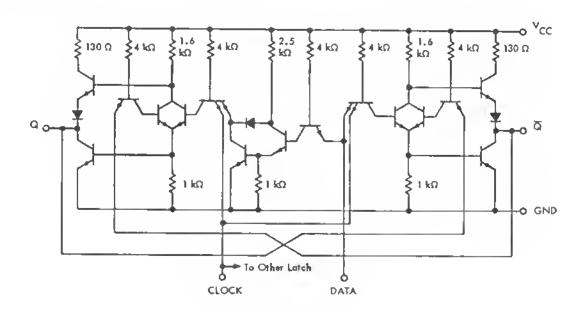
Rev.

Sheet - of

functional block diagram (each latch)



schematic (each latch)



THE FOXBORO COMPANY B V3008 FA

- 5039 (6/68)

recommended o	perating con	ditions																												
Su	pply Voltage V	сс ⁽⁵⁰⁰	Not	N 1)																					4	.75	v	to	5.25	v
Fa	n-Out From Ou	tputs	٠.																										T to	10
absolute maxim	num ratings o	over op	era	ting	fr	ee.	-ai	r te	em	per	ati	uri	er	an	qe	(u	nlı	PS 5	ot	he	rw	156) r	ot	eď					
Suj	pply Voltage V _C	C (200	Noh	e 1)																									. ,	v
Ing	out Voltage V	(See No	of the	Tana	1 2)																								5.5	v
Op	erating Free-Ai	ic Tempe	ratu	re Ro	ngi	٠.																					0"	٠.	ላ ጀመ	ے.
MOTES: 1" IL	rage Temperatu tese voltage volt put tignals must	Ues Ore 1	with	resp	out	to	net	wor	kα	rou	nd 1	terr	min	ol.						•	•	•	•	•	1	~55)"C	ю	150	"C
electrical chara	cteristics. T	A * 0°(C to	70°	C (ในก	iles	22	oth	61	WİS	e	no no	tec	nd ()	ren	ni n	ol,												

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN T	YP MAX	UNIT
V _{in(1)}	Input voltage required to ensure logical Lilevel at any Input terminal	Т	∨ _{CC} =4.75 ∨	2		٧
V _{In(0)}	input voltage required to ensure logical () level of any input terminal	2	V _{CC} =4,75 V		0,8	v
V _{out(1)}	Legical Toutput voltage	and 2	V _{CC} =4,75 V, I _{local} = -400 µA	2.4	-	v
V _{out (0)}	Legical O autput valtage	ond 2	V _{CC} =4.75 V _± 1 _{sink} =16 mA		0.4	٧
I _{In(0)}	Logical O level Input current of D	3	V _{CC} =5.25 V, V _i =0.4 V		-3.2	mA
in(0)	Logical D level Input current at clock	3	V _{CC} =5.25 V ₁ V _{In} =0.4 V		-6.4	mA
in(1)	Logical 1 level Input current of D	3	V _{CC} =5.25 V ₁ V _{1n} =2.4 V V _{CC} =5.25 V ₁ V _{1n} =5.5 V		80	μA mA
l _{in(1)}	Logical Tlevel Input current at clack	3	V _{CC} =5,25 V, V _{1n} =2,4 V V _{CC} =5,25 V, V _{1n} =5,5 V		160	μĀ mA
los	Short-circuit output	4	V _{CC} =5,25 V, V _{DU1} =0	- T8	-57	mA
I _{CC}	Supply current	5	V _{CC} =5 V ₊ T _A =25°C	3	2	mĀ

T Not more than one output should be shorted at a time. switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	FIGURE	TEST CONDITIONS	MtM	TYP	MAX	וואט
setup l	Minimum logical 1 level Input setup time at 0 input	5A	$C_L = 15 \text{ pF, } R_L = 400 \Omega$		7	20	m
setup0	Minimum logical 0 level input setup time at D input	5A	C _L = 15 pF, R _L = 400 Ω		14	20	l'Hi
holdl	Maximum logical Flevel input hold time required at D input	5A	C _L = 15 pF _s R _L = 400 Ω	0	T5 🕴		m
hold()	Maximum logical D level input hald time required at D input	5A	$C_{L} = 15 \text{ pF}_{H} R_{L} = 400 \Omega$	0	61		ne
pd1(0-Q)	Propagation delay time from D input to Q output	5A	C ₁ = 15 pE ₁ R ₁ = 400 Ω	1	T6	30	THE
pd0(D-Q)	Propagation delay time from D input to Q output	5A	C _L = 15 pF _± R _L = 400 Ω		14	25	nt
pd1(D-Q)	Propagation delay time from D input to Q output	5A	C _L = 15 pF, R _L = 400 Ω	1	24	40	T(d)
pd0(D-Q)	Propagation delay time from D input to Q output	5A	C _L = 15 pF, R _L = 400 Ω		7	15	rts
pd1(C-Q)	Proposation delay time from clock input to O output	5A	$C_{L} = 15 \text{ pF}_{B} R_{L} = 400 \Omega$		Tá	30	ns.
	Propagation delay time from clock innut to O output	5A	C _L = 15 pF _s R _L = 460 Ω		7	T5	กเ
	Propugation delay time from clock input to Q output	5A I	C _L = 15 pF _a R _L = 406 Ω	1	16	30	m
pd0(C−Q)	Propagation delay time from clock input to Q output	5A	C _L = 15 pF _a R _L = 400 Ω		7	15	ms

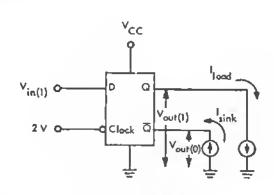
[†] These typical times Indicate that period occurring prior to the T_s5 V level at clack pulse t₀ during which date at the D input will still be recognized.

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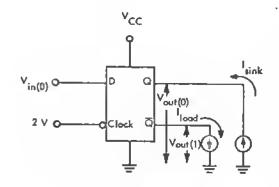
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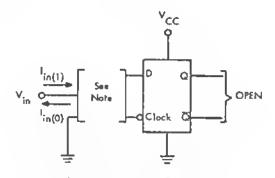
1. Each output is tested separately,

FIGURE 1



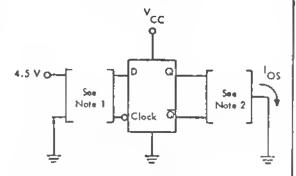
1. Each output is tested separately.

FIGURE 2



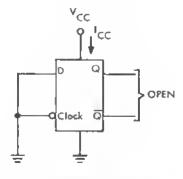
- Each Input is tested separately.
 When testing l_{in(1)} at D ground clock.
- 3. When testing I in(1) at clock ground all D inputs.

FIGURE 3



- 1. Input conditions are in accordance with truth table depending on output under test.
- 2. Each latch and each input is tested separately.

FIGURE 4



1. All forches are tested simultaneously,

FIGURE 5

‡ Arrows indicate actual direction of current flow.

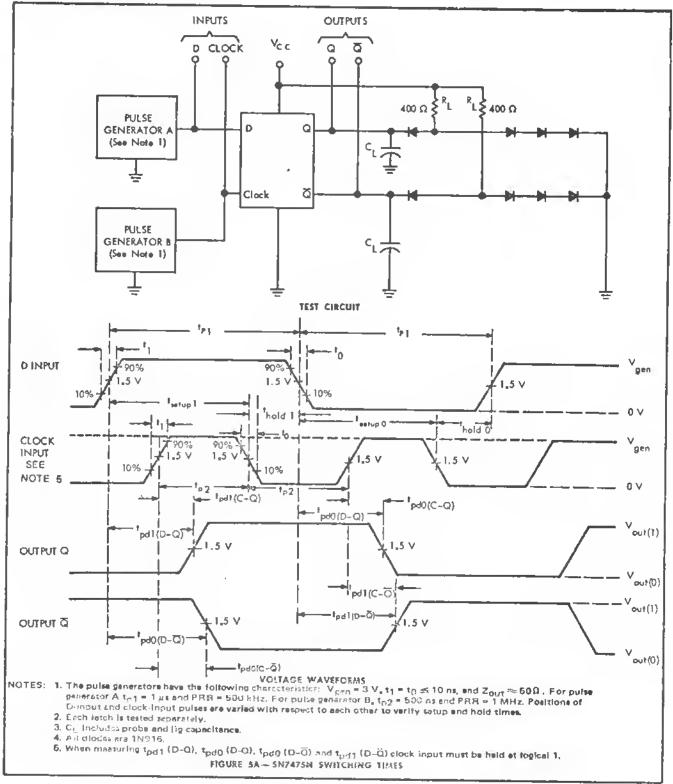
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Sheet

PARAMETER MEASUREMENT INFORMATION

switching characteristics



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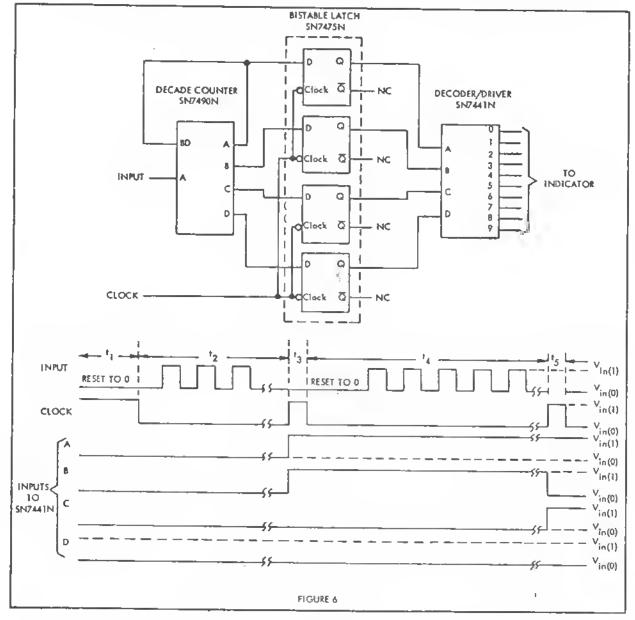
temporary storage of binary data

This application demonstrates the use of the SNJ475N bistable latch as a temporary storage of binary-coded decimal data, from the SNJ490N decade counter, which is to be decaded by the SNJ441N decader/driver. Temporary storage is desirable at this point for two reasons:

- a. At counting frequencier above several cycles per second, it is sometimes desirable to eliminate the flicker on the display tube caused by reading an input count which is too fast to be recognized.
- During the time that the latch is storing information the decade counter may start acquiring data for the next display.

A typical sequence of operation is illustrated (see figure 6):

- 1. During $t_{1\pi}$ reset decade counter to 0. At and of $t_{1\pi}$ indicator will display "0".
- 2. During 12x count BCD 3 at output of SN7490N. Indicator still displays "0".
- At start of t₃, indicator will display "3". At end of t₃, BCD 3 is committed to memory by 5N7475N and the 5N7490N may begin counting again.
- During t₄, reset decade counter to 0 and count 8CD 5 at output of SN7490N. Indicator still displays "3" -
- At stort of t₅, indicator will display "5". At end of t₅, BCD 5 is committed to memory by SN7475N and the SN7490N is released......



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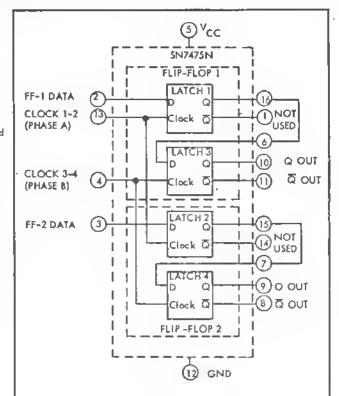
TYPICAL APPLICATION

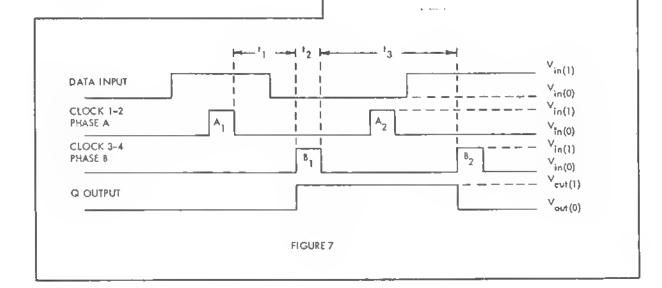
dual D-type master-slave flip-flop

This application demonstrates the use of the SN7475N as a dual D-type master-slave flip-flop, provided that two-phase clocking is permissible. Each af the D-type flip-flops are formed by merely interconnecting the O autput of one of the latches (which serves as the moster) to the data input of another latch (which serves as the slave). Each of these interconnected latches must have a separate clock line; therefore if a dual D-type master-slave flip-flop is constructed from a single package (see figure 7) they must be operated synchronously.

A typical transfer of data is illustrated. Note that after the start of t_1 the data input is released to acquire new information as the master section has "lacked up" the original data after clack pulse A_{1} . At the start of t_2 the data "lacked up" in the master is transferred to the autput, and at the end of t_2 (and for the duration of t_3) the slave retains the original data.

This type of flip-flop is desirable in applications where speed is not a primary requirement and where the additional clock skew, resulting from this delay between the twa clock pulses, affards greater system reliability.





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FIRST USED ON		REVISIONS	-		
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I	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

FURM SDSSA (S/ST)

Circuit, Integrated (Dual In-Line Package)
Dual Master/Slave Flip-Flop with Pre-Set and Clear

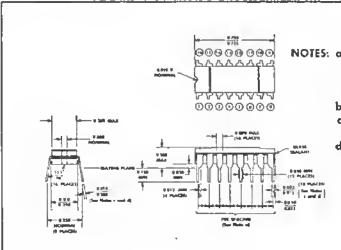
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 4
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7476N Sprague Part No. USN7476B National Semiconductor Corp. Part No. OM8500N Motorola Part No. MC7476P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT NLESS OTHERWISE SPECIFIED WORK AUTH NO. THE FOXBORO COMPANY MOVE BURRS & SHARP EDGCS FOXBORO, MASSACHUSETTS, U.S.A. B Washer PATE - HENDICKE AND IN INCHES IL DIN'S APPLY AFTER PLATING TITLE: DESIGHER CIRCUIT, INTEGRATED . LERALGES ON DUAL IN-LIME PACKAGE GACTIONS: ± 1/64 CHECKER ACIMALS # .005 TYPE SN7476N 領令1製造ご子 Jula Dena MATERIAL: SIZE SYMBOL DRAWING NO. REV RELEASEL Α FINISH: SCALE: NONE LOCAL RELEASE SHEET I OF 4

A



NOTES: a. The true-position pin spacing is 0.100 between conterlines. Each pin centerline is lacated within ±0.010 af its true longitudinal position relative to pins 1 and 16

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

16-PIN FUNCTIONS

THE FOXBORO COMPANY SYSTEMS DIVISION

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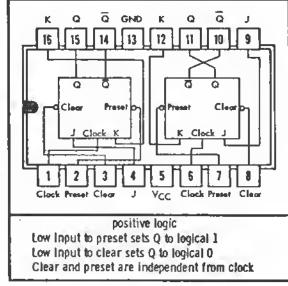
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Sheet 2 of 4

TRUTH TABLE											
e,	t _n										
j	K	Q									
0	0	G,									
0	1	Ð									
1	0	1									
1	1	Ġ,									

NQTES:

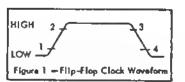
- 1. t_n = Sit time before clock pulse.
- t_{n+1} = Sit time after clock pulse.



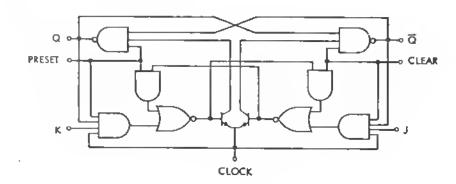
description

The SN7476N J-K filp-flop is based on the master-slove principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see figure 1):

- 1. Isolate slave from master
- 2. Enter information from J and K inputs to master
- 3. Disable J and K Inputs
- 4. Transfer Information from master to slave.



functional block diagram (each fllp-flop)



THE FOXBORO COMPANY SYSTEMS DIVISION

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Rev.

Sheet 3 of 4

recommended operating conditions

Supply Valtage V _{CC}	٧
Fan-Out From Each Output, N	10
Wildth of Clock Pulse _s t _p (clock) · · · · · · · · · · · · · · · · · · ·	
Width of Clear or Preset Pulse ≥ 25	
Input Setup Time, testup	th
Input Hold Time, hold	

electrical characteristics, TA = 0°C to 70°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	זואט
V _{In(1)}	Input voltage required to ensure logical 1 at any input terminal	V _{CC} = 4.75 V	2			٧
V _{In(0)}	Input voltage required to ensure logical 0 at any Input terminal	V _{CC} = 4.75 V		_	0.8	٧
Vout(I)	Logical 1 output voltage	V _{CC} = 4.75 V, t _{lood} = -400 μA	2.4	3.5		٧
Vout (0)	Logical 0 output valtage	VCC = 4.75 V, Islak = 16 mA		0.22	0.4	V
l _{ln} (0)	Logical O level input current at J or K	V _C C = 5.25 V _s ∀ _{ln} = 0.4 ∨			-1.6	mA
[[] {n(0)	Logical O level Input current at clear, preset, or clock	V _{CC} = 5.25 V, V _{In} = 0.4 V			-3,2	mА
l _{[n(1)}	Logical 1 level input current at J or K	V _{CC} = 5.25 V _s V _{in} = 2.4 V V _{CC} = 5.25 V, V _{in} = 5.5 V			40	μA mA
lin(1)	Logical 1 level Input current	V _{CC} = 5.25 V _s V _{in} = 2.4 V			80	μA
-in(i)	at clear, preset, or clock	V _{CC} = 5.25 V, V _{In} = 5.5 V			1	mA
los	Short-circuit output currentt	V _{CC} = 5.25 V, V _{in} = 0	-18		-57	mA
l _{CC}	Supply current (each flip flop)	VCC = 5 V, Vln = 5 V		В		mΑ

†Not more than one output should be shorted at a time. These Typical values are at VCC = 5 V, and TA = 25°C.

switching characteristics, V_{CC} = 5 V, TA = 25°C, and N = 10

_	PARAMETER	1EST CONDITIONS	MIN	TYP	MAX	UNIT
felock	Maximum clock frequency	C ₁ ≈ 15 pF	10	15		MHz
l _{pd1}	Propagation delay time to logical O level from clear or preset to output	C ₁ = 15 pF		26	50	ns
f _{pd} 0	Propagation delay time to logical I level from clear or preset to autput	C ₁ = 15 pF		34	50	ris
†pd1	Propagation delay time to logical 1 level from clock to output	C ₁ = 15 pF	10	25	50	,nst
¹pd0	Propagation delay time to logical O level from clock to output	C ₁ = 15 pF	10	34	50	ns

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Α	LOCAL	RELEASE	ECN	NO. 1917.			

1. DESCRIPTION

FIRST USED ON

4- 0088A (4/47)

Circuit, Integrated (Dual In-Line Package) Full Adder

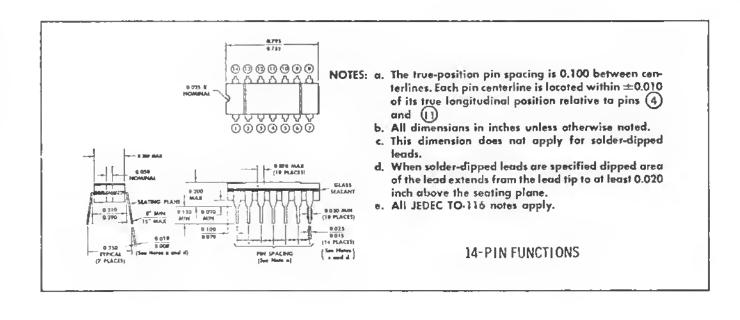
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheets 5,6,7,8,9,10 & 11
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7480N Sprague Part No. USN7480A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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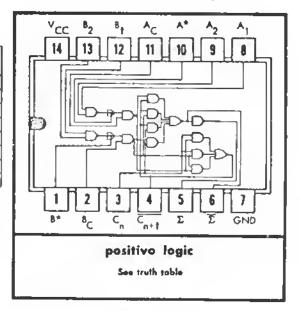
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TRUTH TABLE (See Notes 1, 2, and 3)

c,	•	A	C _{n+1}	E	2
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	G	1	0
1	0	0	1	0	ī
1	0	1	0	"1	G
1	1	0	0	1	0
1	1	1	0	0	1

NOTES: 1. $A = \overline{A + A_c}$, $B = \overline{B + B_c}$ when $A + \overline{A_1 + A_2}$, $B + \overline{B_1 + B_2}$

- 2, When AN or BN are used as input; A₂ and A₂ or b₁ and b₂ respectively must be connected to GHD;
- 2. When A, and A2 or B, and B2 are used as laputs, A4 or 84 respectively must be agen or used to perform 9at-O2 legic,



description

The SN7480 is a single-bit, high-speed, binary full adder with goted complementory inputs, complementary sum (Σ and Σ) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parollel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diade-transistar logic (DTL) for the gated inputs, and high-speed, high-fon-out transistar-transistar logic (TTL) for the sum and corry outputs. The circuit is entirely compatible with bath DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained cansiderably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

recommended oporoting conditions

Supi	ply Voltage Vcc													٠	٠		٠	4.7	5	V ta	5.25	٧
Max	imum Allawable	Fan-	-Out	Fra	m	Οu	tpu	ts:														
	$\overline{C_{n+1}}$, N								٠							٠	٠				1 ta	5
	Σ or $\overline{\Sigma}$, N																				1 to 1	10
	A* ar B*, N .																				1 10	3

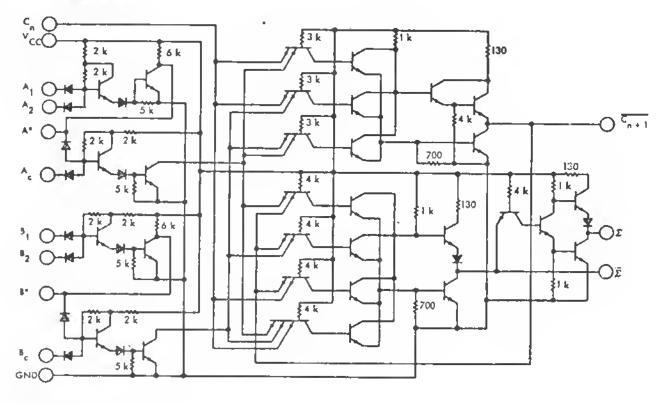
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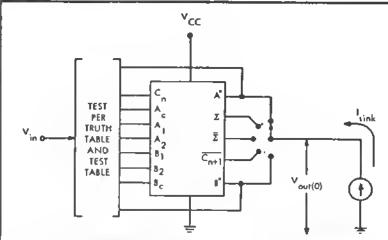
schematic diagram



Component volves shown are naminal, Resistor values are in ahms,

THE FOXBORO COMPANY V3008 FC

d-c test circuits § (continued)

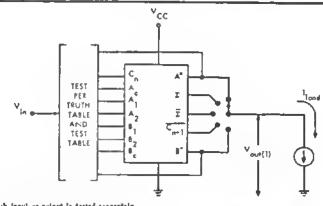


TEST TABLE

1231 TAB	A E
Output Under Test	I _{alrik} (Rin)
N or N	16 mA
Ç _{n+1}	I mA
A木 or B木	4.0 mA

-). Each laput or unique is lasted separately.
- 2. When A% is instead A_1 and A_2 are at GRD. When B% is lested B_2 and B_3 are at GRD,
- 3. When \mathbb{A}_1 and \mathbb{A}_2 or \mathbb{B}_1 and \mathbb{B}_2 is insteal, $\mathbb{A} \#$ or $\mathbb{B} \#$ respectively, is open.

FIGURE 42



TEST TABLE

Dulput Under Test	I _{load} (Sin)
Σ κ Σ	- AUL COP-
Ç ₁ + 1	+200 μA
A 東 10 B 中	-120 µk

- 1. Each input or sulput is tested separately.
- 2. When AR is lested A1 and A2 are al GHD, When BR is tested B2 and B3 are al GHD,
- 3. When A, and Ag or By and By are tested Art or Brit, respectively, is open,

FIGURE 43

SArrows Indicate actual direction of correct flow.

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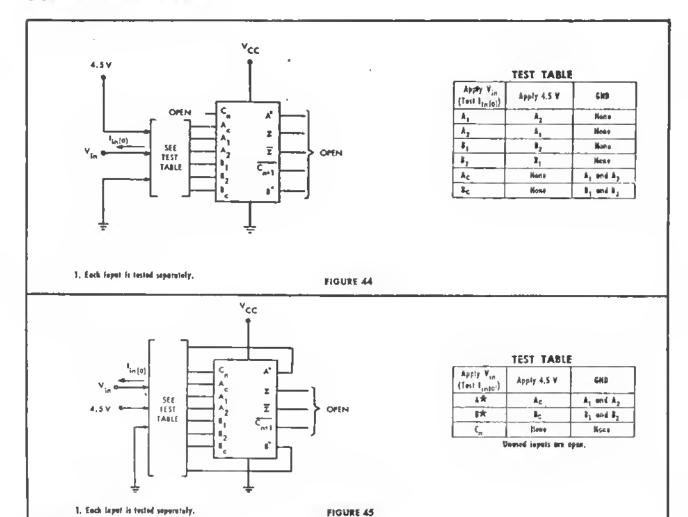
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of

d-c test circuits (continued)



SArrows Millerte actual direction of current flow.

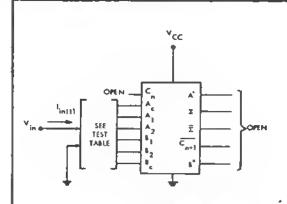
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V3008 FC

| Sheet = of | 1

d-c test circuits (continued)

CAN'T Day 1 . Type



1. Each Input is tested separately.

TEST TABLE

Apply V _{in} (Test i _{m(1)})	6N3
A	A ₂
Ay	A ₁
¥ ₁	R ₂
1 2	l ₁
Ac	A#
li _c	17

FIGURE 46

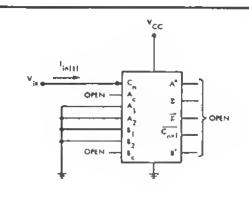
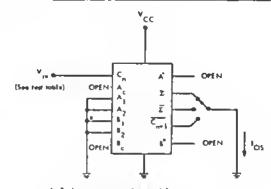


FIGURE 47



1. Each aniput is tested superately.

TEST TABLE

Output Under Tust	V _{in} Value
	V _{CC}
∑ er C _{1 + 3}	CHD

FIGURE 48

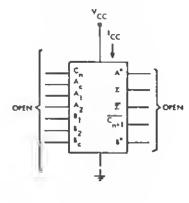


FIGURE 49

SAmens ludicate octout direction of current flow,

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Rev.

electrical characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$

PARAMETER		TEST FIGURE	TEST CONDITIONS I		TYP MAX	זומט
Y _{ir(1)}	Logical 1 input voltage	/2 and 43	$V_{CC} = 4.75 \text{ V}, V_{en(0)} = 0.8 \text{ V}$ $V_{out[1]} \ge 2.4 \text{ V}, V_{out[0)} \le 0.6 \text{ V}$			٧
Y _{in(0)}	Logical O input valtage	42 and 43	$V_{CC} = 4.75 \text{ V}, V_{in[1]} = 2 \text{ V}, \\ V_{out[1]} \ge 2.4 \text{ V}, V_{out[0]} \le 0.4 \text{ V}$	/	0.8	٧
V _{00+[1]}	Lagical 1 autput voltage	43	V _{CC} = 4.75 V	2.4	3.5‡	V
V _{out 0)}	Lagical O autput voltage	42	V _{CC} = 4.75 V		0.22‡ 0.4	V
l _{in(0)}	Logical O level input current at A ₁ , A ₂ , B ₁ , B ₂ , A _c ar B _c	44	$V_{CC} = 5.25 V$, $V_{in} = 0.4 V$		-1.6	mA
l _{in(0)}	Logical O level input current at A× ar B×	45	V _{CC} = 5.25 V, V _{In} = 0.4 V		-2.6	mA
l _{in[0]}	Lagical O level input current at C _n	45	$V_{CC} = 5.25 V_e V_{in} = 0.4 V$		- 8	mA
l _{och)}	Logical 1 level (nput current at A ₁ , A ₂ , B ₁ , B ₂ , A ₄ or B ₄	46	$V_{CC} = 5.25 \text{ V}, V_{cn} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{cn} = 5.5 \text{ V}$	-	15	μA mA
l _{iolij}	Logical 1 level input current	47	$V_{CC} = 5.25 V_{r} V_{ra} - 2.4 V_{ra}$		200	μA
los	at C _n Shart-circuit autput current at \sum ar \sum †	4B	$V_{CC} = 5.25 \text{ V}, V_{in} = 5.5 \text{ V}$ $V_{CC} = 5.25 \text{ V}$	-18	- 57	mA mA
102	Shart-circuit autput curient at C _{n+1} †	48	V _{CC} = 5.25 V	-18	-70	mA
Icc	Supply current	49	V _{CC} - 5 V		21‡	mA

That more than one output should be shorted at a time,

\$These typical values are at $Y_{\rm CC}=3$ Y, $T_{\rm A}=25^{\rm o}{\rm C}$.

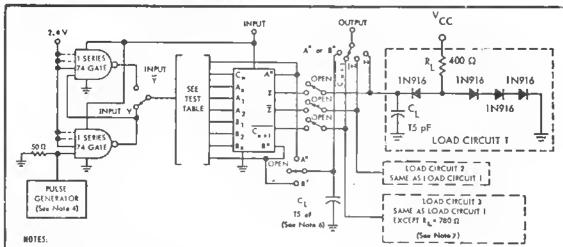
switching characteristics, $V_{\text{CC}} = 5\,\text{V}, T_{\text{A}} = 25\,^{\circ}\text{C}$

PARAMETER ¶	FROM INPUT	TO OUTPUT	FIGURE 57 TEST NO.	TEST CONDITIONS	MIN TYP	MAX	UNIT
1 _{pd1}	C,	Č _{n+1}	1	N = 5	13	17	ns
f _{pd0}		-n+1	2	N = 5	8	12	n)
† _{pd1}	8 _C	C _{n+1}	3	N = 5	18 .	25	ns
† _{pd0}	~c	-n+1	4	N = 5	38	55	Πs
† _{pd1}	Ac	Σ	5	N = 10	52	70	ns
pd0	~¢ .		6	N = 10	62	80	ns.
1 _{pd1}	Bc	<u>z</u>	7	N = 10	38	55	ns
†pd0			8	N = 10	56	75	ns
1 _{pd1}	A _i	A*	9	$C_L = 15 pF$	48	65	ns.
† _{pd8}	- 1		10	$C_L = 15 \text{ pF}$	17	25	ns
† _{pd1}	8,	8*	11_	$C_L = 15 pF$	48	65	DS
pd0	Y1	"	12	$C_L = 15 pF$	17	25	ns

 $\mathbf{1}_{\mathrm{pd1}}$ is proposation delay time to logical 1 level, t_{pd0} is proposation delay time to logical 8 level,

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switching characteristics (continued)



- I. Perform feel in accordance with lost table,
- 2. Each output is tosted separately.
- 3. Voltage values are with respect to network GHD terminal;
- 4. The generalor has the following characteristics: $Y_{\rm quer}=3$ V, $t_{\parallel}=t_0\leq$ 15 ms, $t_p=0$ S μ_1 , PBR =-1 MHz, and $X_{\rm out}\approx$ 50 ST.
- 5. Inputs and outputs not otherwise specified ore open,
- $\theta \in C_L$ and $C_{\tilde{q}}$ include probe and jig capacitance,

TEST CIRCUIT

7. Lood circuit 2 stessioler appart food of 5.

PULSE	7. 90%	90%	* †o
GENERATOR OUTPUT	50%	Tp 50%	10%
_	\ !		!/-

ı	63	1 1	24.0	3 LE	43	44	N	916	-5)
	Т	APP	LY	Т			Т		

TEST NO.	OUTPUT UNDER TEST	APPEY IMPUT Ÿ IO	Y TURKI OT	APPLY + 2.4 V TO	APPLY GND TO	OUTPUT EQUATING TO
1	Ç,+1	hone	ζ,	Neha	R ₁	$\overline{C_{n+1}}$ (N = 5)
1	C+1	Hose	(_n	Name	0,	ζ_{n+1} ($z = s$)
1	ζ_{n+1}	6 g	None	ζ,,	4,, 0,	$\overline{\zeta_{n+1}}$ (N = 5)
4	Ç ₁₊₁	O _D	liane.	€ _n	$A_1,\ B_1$	$\zeta_{n+1} = \{n = s\}$
5	Σ	Ac	N'ene	Ç _n	A ₁ , B ₁	$\frac{\Sigma}{\Sigma} (N = 10)$ $\frac{\Sigma}{\zeta_{n+1}} (N = 5)$
6	Z	A _e	None	Ç	A ₁ , B ₁	$\frac{\Sigma}{\Sigma} (\aleph = 10)$ $\frac{\Sigma}{C_{n+1}} (\aleph = 5)$
7	Σ	0 _c	Risco	(,,	¥,	½ (M = 10)
4	Z	II.	Read	ζ,	B ₁	[6T = K) Z
7	Ack	Kens	ű,	A ₂	Nana	λ★ (ζ _L = 15 / 5)
10	ÁΨ	Kans	A	Ay	Чила	λ ^{(ξ} (ξ ₁ = 15 μξ)
11	■液	Itens	d ₁	1,	Rome	$(C_1 = 15 \text{ pF})$
12	8 W	Fore	R ₁ ·	2,	Pose	$\xi^{*}\ell = (\xi_{ij} = 15 \text{ pF})$

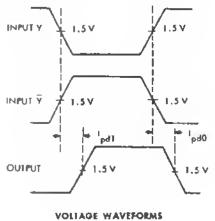


FIGURE 37 - SN7 171 SWITCHING TIMES

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TYPICAL APPLICATIONS

n-bit binary adder or subtractor (see figures F and G)

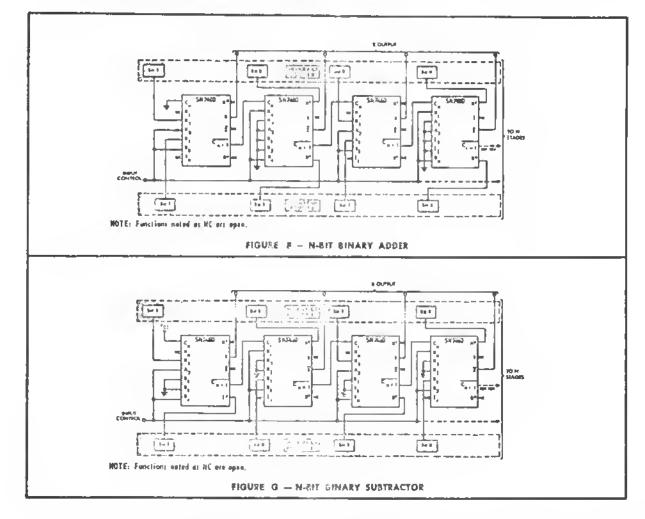
The SN7480 is designed specifically for N-bit adder or subtractor aperations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clack rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is sa slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the corry delay. The corry circuit employs a high-speed Darlington output, and the logic goting has only one inversion between the C_n input and the $\overline{C_{n+1}}$ output. This logic configuration results in an inverted carry autput, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B Inputs and the resulting sum or difference output. This

interconnection method is illustrated by bit 2 and bit 4 of the odder ffigure F). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

When performing subtraction (figure G) the $C_{\rm e}$ input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (figure F), input control is applied to A_2 and B_2 of odd-numbered bits and to A_c and B_c of even-numbered bits. For the subtractor (figure G), input control is applied to A_2 and B_c of the odd-numbered bits and to A_c and B_c of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



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APPLICATIONS

n-bit binary adder with register selection (Ac. 1 = a H

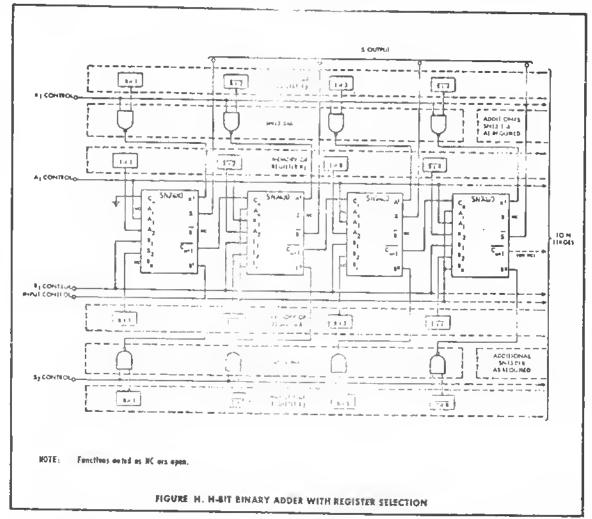
This opplication fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single odder for each bit required. Register selection is performed internally for registers A₁ and B₁ and externally by a type SN15 846 DIL gate for registers A₂ and B₂. Dat-OR logic is performed at the A* and B* nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register A₁ to Register B₁, A₂ and B₂ control lines are brought to the logical 0 state. (If the input to these lines is from a logic gate, fon-out rules should be observed.) In the foshion, the contents of register A₁ are added to to the B₂ by holding A₂ and B₁ control lines at a logical form register combinations may be used. Even numbered input bits from each register must be inverted since the A* and B* inputs are being used to perform Supply logic. This is not a configuration restriction for figurapy type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in figure H. Inputs from the register-control gates (SN15-845) of the additional registers would be Dot-OR connected with A₂ and B₃ registers at the A* and B* Inputs,

To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control temples the same.



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FIRST USED ON		REVISIONS			
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•	A	LOCAL RELEASE ECH NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
2-Bit Binary Adder

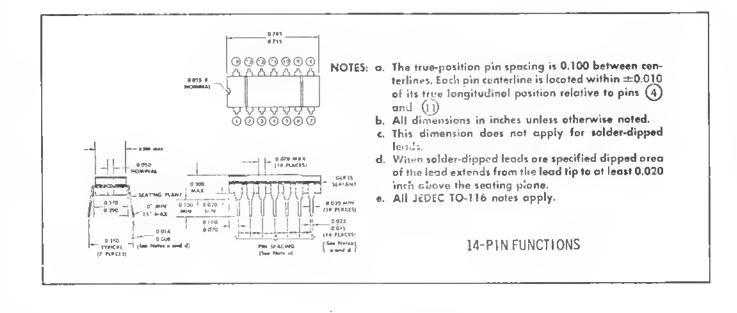
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheets 4,5,6,7,8 & 9
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN74B2N Sprague Part No. USN74B2A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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THISH: 1	RELEASE	4/10/15	SIZE SYMBOL DE	RAWING NO. V3008FE A
	LOCAL RELEASE		SCALE: NOTE	SHEET I OF S

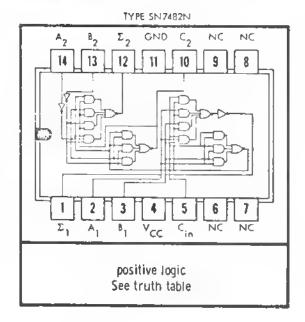


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Sheet 2 of 1



logic

TRUTH TABLE

	INI	UT				OUT	PUT		
				WHE	N C _{In}	= 0	WH!	EN C _{in}	= 1
A ₁	81	A 2	82	Σ	Σ2	C ₂	Σ	Σ2	C ₂
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	ı	0	0	Ŀ	0	0	0	1	Ò
1	1	. 0	0	0	ı	0	1	. 1	0
0	0	1	0	0	1	٥	1	1	0
1	0	1	0	1	ı	0	0	0	1
0	1	1	0	1	!	0	0	0	ı
1	1	1	0	0	0	1	1	0	1
0	0	٥	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	_1	0	1	0	0	L	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1.	1
1	1	1	1	٥	1	1	1	1	1

description

This full adds: performs the addition of two 2pbit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for mealum-ta-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-speed, high-speed, high-speed, bit from the control of the implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lock-ahead" and carry-coscoding circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

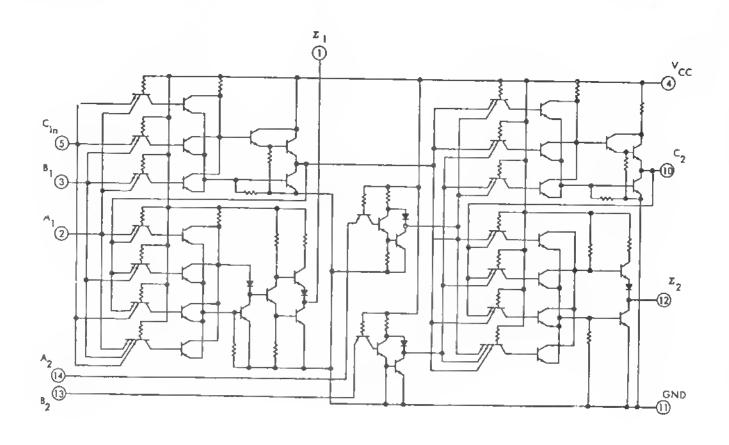
THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 3 of 9

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switching characteristics. V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

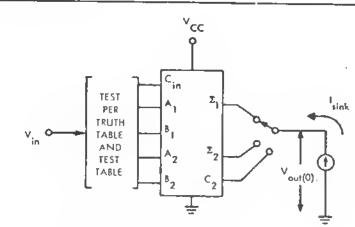
PARAMETER 1	FROM (INPUT)	TO (OU1PUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN TYP	МАХ	UNIT
[†] pd l	,	*	1			34	ns
Pd0	C _{in}	Σ1	2			40	134
†pd1	D	7	3			40	ns
t pd0	^B 2	Σ2	4		_	35	ns.
†pď l		7	5			38	ns
† pd0	Cin	Σ2	6			42	ns
t _{pd} 1	٠		7	N = 5	17	27	ns
† _{pd} 0	C _{in}	c ₂	8	N = 5	12	19	P) S

If t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

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d-c test circuits t

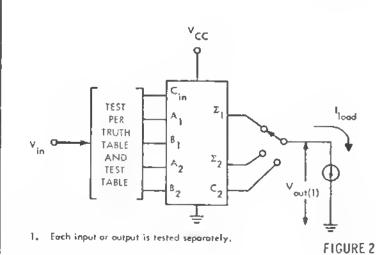


TEST TABLE

OUTPUT UNDER TEST	sink
Σ_1 or Σ_2	16 mA
C ₂	B mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

OUTPUT UNDER TEST	lood
Σ_1 or Σ_2	— 400 µA
c ₂ .	−200 µA

fArrows indicate actual direction of current flow,

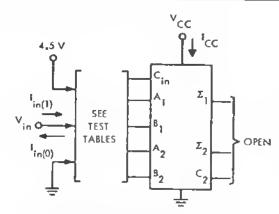
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5039 (6/23)

d-c test circuits + (continued)

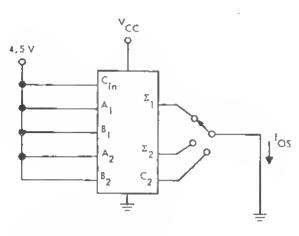


I _{in(0)} I	EST TABLE
APPLY V in TEST I	APPLY 4.5 V
Cin	A ₁ and B ₁
. A ₁	Cand B
В ₁	C and A
A ₂	None
В	None

in(1) TE	ST TABLE
APPLY V in	GND
C _{in}	A ₁ and B ₁
A ₁	C and B
B ₁	C _{in} and A ₁
A ₂	None
B ₂	None

- 1. Each input is tested separately.
- When testing ICC apply 4.5 V to A₁, A₂, and C_{Int} and ground 8₁ and B₂.

FIGURE 3



1. Each output is tested separately.

FIGURE 4

throws indicate actual direction of current flow.

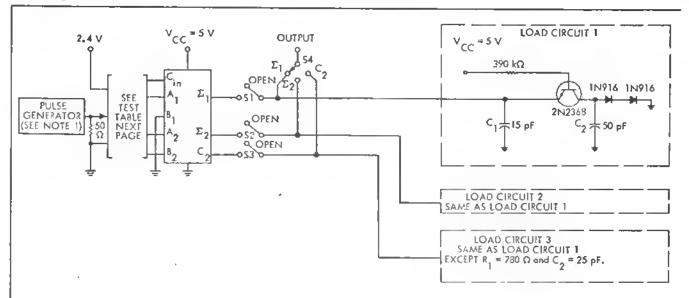
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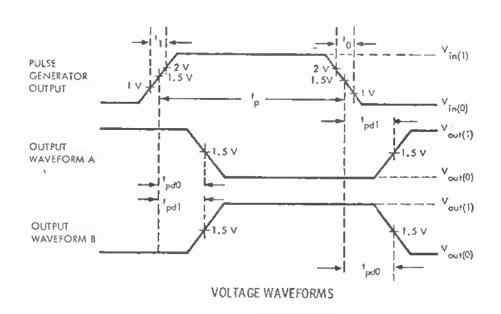
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Rav.

switching characteristics



TEST CIRCUIT



NOTES: 1. The generator has the following characteristics: $V_{in(1)} \ge 2.4 \text{V}$, $V_{in(0)} \le 0.4 \text{ V}$, $t_1 = 8 \text{ to } 15 \text{ ns}$, $t_0 = 3 \text{ to } 5 \text{ to }$ PRR = 1 MHz, t = 200ns, and Zout \approx 50 Ω_{\star}

- 2. Perform test in accordance with test table.
- 3. Each output is tested separately.4. Valtage values are with respect to network ground terminal.
- 5. C₁ includes probe and jig capacitance.

FIGURE 5. SWITCHING TIMES

THE FOXBORO COMPANY SYSTEMS DIVISION Sheet

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V _{CC} (See Nota 1)			٠																7 V
Input Voltage V _{In} (See Notes 1 and 2)			٠					٠											5.5 V
Operating Free-Air Temperature Range																			
Storage Temperature Range (SN7482)	٠	٠		٠	٠		٠					٠		٠		-	.65°	'C to	150°C
Storage Temperature Range (SN7482N)							٠			٠						-	·55°	'C to	125°C

NOTES:

- T. These voltage values are with respect to network ground terminal.
- 2. Input signals must be positive with respect to network ground terminal

recommended operating conditions

Supply V	altage	V _C	۲.	٠						٠				٠						 4.	75	V to	5.25 V
ron-Our	rrom (July	oun;																				
c ₂ .		٠				٠		٠		٠	٠				٠								1 to 5
Σ ₁ or																							

electrical characteristics, $T_A = 0$ °C to 70°C

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN TYP	мах	TIMU
V _{in(1)}	Input voltage required to ensure logical) at any input terminal	1 and 2	V _{CC} = 4.75 V	2		V
V _{In(0)}	toput valtage required to ensure logical 0 at any input terminat	i and 2	V _{CC} = 4.75 ∨		0.8	
V _{∞t(1)}	Logical 1 output voltage	2	V _{CC} = 4.75 V	2.4		V
V _{out(0)}	Logical 0 output voltage	1	V _{CC} = 4.75 V		0.4	٧
(0,n; ³)	Logical O level input current of A ₁₁ B ₁₁ or C _{in}	3	$V_{CC} = 5.25 \text{V}, V_{in} = 0.4 \text{V}$		-6,4	mΑ
I _{In(0)}	Logical O level input current of A ₂ or 8 ₂	3	$V_{CC} = 5.25 \text{ V}. V_{in} = 0.4 \text{ V}$		-1.5	mΑ
l _{in(1)}	Logical 1 level input current of A ₁ , B ₁ , or C _{in}	3	$V_{CC} = 5.25 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{in} = 5.5 \text{ V}$		160	μA mA
lin(I)	Logical 1 level input current at A ₂ or B ₂	3	$V_{CC} = 5.25 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.25 \text{ V}, V_{in} = 5.5 \text{ V}$		<u>40</u> 1	μA mA
¹ 05	Short-circuit output current of Σ_1 or Σ_2 ?	4	∨ _{CC} = 5.25 ∨	-18	-55	mA
los	Short-circuit output current of C2 [‡]	4	V _{CC} = 5.25 V	-18	-70	πΑ
l _{cc}	Supply Current	3	V _{CC} = 5 V, T _A = 25°C	35		mA

1Not more than one cutput should be shorted at a time.

THE FOXBORO COMPANY SYSTEMS DIVISION

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Asnest F of

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V _{CC} (See Note 1)														-											7 V
Input Voltage V (See Notes 1 and 2)																									5,5 V
Operating Free-Air Temperature Range Storage Temperature Range	:	:	:	:	:	:	:	:	:	:	:	:	:		:			:	:			-	-55°	IC N	o 125°C
NOTES										,	-	-	-	-	-	-	-	-	-	-	•				

1. These valtage values are with respect to network ground terminal.

2. Input signals must be positive with respect to network ground terminal.

recommended operating conditions

Supply Valtage V _{CC}										÷	,						4.5	i V i	6 5,5 V
Fon-Out From Outputs:																			
c ₂		•			ph								-					-	1 to 5
Σ_1 or Σ_2																			1 to 10

electrical characteristics, T_A = 55°C to 125°C

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN TYP	MAX	זואט
V _{in(1)}	Input voltage required to ensure lagical 1 at any input terminal	1 and 2	V _{CC} = 4.5 ∨	2		٧
V _{in(0)}	Input voltage required to ensure lagical 0 at any input terminal	1 and 2	V _{CC} = 4.5 ∨ .		0.8	V
V _{out(1)}	Logical 1 output voltage	2	V _{CC} = 4.5 ∨	2.4		٧
V _{pu1} (0)	Logical O pulput voltage	1	V _{CC} = 4.5 V		0.4	٧
¹ in(0)	Lagical O level input current of A ₁ , B ₁ , or C _{in}	3	∨ _{CC} = 5.5 V. ∨ _{in} = 0.4 V		~6,4	mΑ
l in(0)	Logical 0 level input current at A ₂ or B ₂	3	V _{CC} = 5.5 V, V _{in} = 0.4 V		-1.6	mA
in(1)	Logical 1 level input current of A ₁ , B ₁ , or C _{in}	3	$V_{CC} = 5.5 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.5 \text{ V}, V_{in} = 5.5 \text{ V}$		160	μA mA
l _{in(1)}	Logical Elevel input current of A ₂ or B ₂	3	$V_{CC} = 5.5 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC} = 5.5 \text{ V}, Y_{in} = 5.5 \text{ V}$		40 1	µА mA
los	Short-cliquit output current of $\Sigma_1^{-\alpha_1}$ or Σ_2^{-1}	4	V _{CC} = 5.5 V	- 20	-55	mA
los	Short-circuit output current of C2 \$	4	V _{CC} = 5.5 V	-20	-70	mA
СС	Supply Current	3	V _{CC} = 5 V , T _A = 25°C	35		mÆ

¹ Not more than one output should be shorted at a time.

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1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
4-Sit Binary Adder

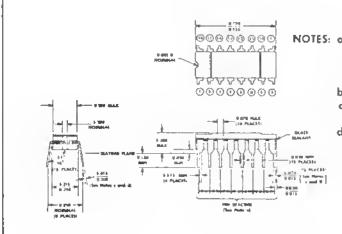
- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheets 5,6,7,8,9 &10
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7483N Sprague Part NO. USN74838

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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VE CURRE & RHARD ETCAR!	WORK AUTH NO.	PAT.	Error S	1.500 10.140	THE FOXBORO COMP	
14 Apply apton blating . U.S. L	octions (<u> </u>	TITES:		T, INTEGRATED	
11 old 1 ± 1/34 11 old 1 ± 1003 1 old 1 ± 1/3*	CHECKET (1) 3 (2) (1)	7/4/1	=		H-LIGE PACKACE TYPE SN74 B3N	
STERIAL: M	MELCALL.	3/24/5	SIZE SY	MBOL O	RAWING NO.	REV
BISH: N			63		VEOUBLE	A
-50224 (0.147)	LOCAL RELEASE		SCALE:	NODE	∫ร∺อยา เ	OFIU



NOTES: o. The true-position pin spacing is 0,100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinol position relative to pins (1) and (18)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not opply for solder-dipped leads.

d. When solder-dipped leads are specified dipped orea of the lead extends from the lead tip to at least 0.020 inch above the seating plune.

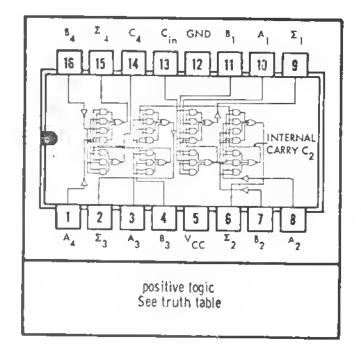
16-PIN FUNCTIONS

THE FOXBORO COMPANY SYSTEMS DIVISION

2 01/0 Sheet

TRUTH YABLE (SEE NOTE 1)

	II-	PUT .				Ou	Put				
				WHEN		15.0]	WHEN C I			
Z	1/,	^2/ /^3	¹ 5/1,	Ξ ₁ /	5/ t,	ς, ς,	ξ ₁ /ε ₁	E3/	7		
0	0	0	Ū	0	0	0	1	0	0		
\perp	٥	<u> </u>	0	_ !	0	0	0	- 6	0		
0	1	0	٥	- 1	0	0	0	I	0		
ı	T	0	0	0	1	٥	1	ı	0		
٥	0		0	0	- 1	0		ı	0		
1	0	I	6	I		0	0	0	$\overline{}$		
٥	1		0	- 1	- 1	0	0	0	1		
		I	0	0	٥	1	1	0	1		
0	0	0		0		0	Ι.	1	0		
1	٥	0		- 1		0	0	0	-		
0		0	1	T		0	0	0	ı		
		0		0	0	Ī	'	0	ı		
٥	0		1	0	0	1	T.	٥	ı		
	٥	1	I	T	0	Τ	0	1	ı		
0	1	1	- 1	Ĭ.	0	T	0	1	1		
		1	i i	0	ı	ı	·	1	1		



NOTE It. Input conditions at A $_1$ A $_2$, B_1 , B_2 , and C_{in} are used to determine autputs Σ_1 and Σ_2 , and the value of the internal corry C_2 . The values at C_2 , A_3 , B_3 , A_4 , and B_4 , are then used to determine autputs Σ_3 , Σ_4 , and C_4 .

description

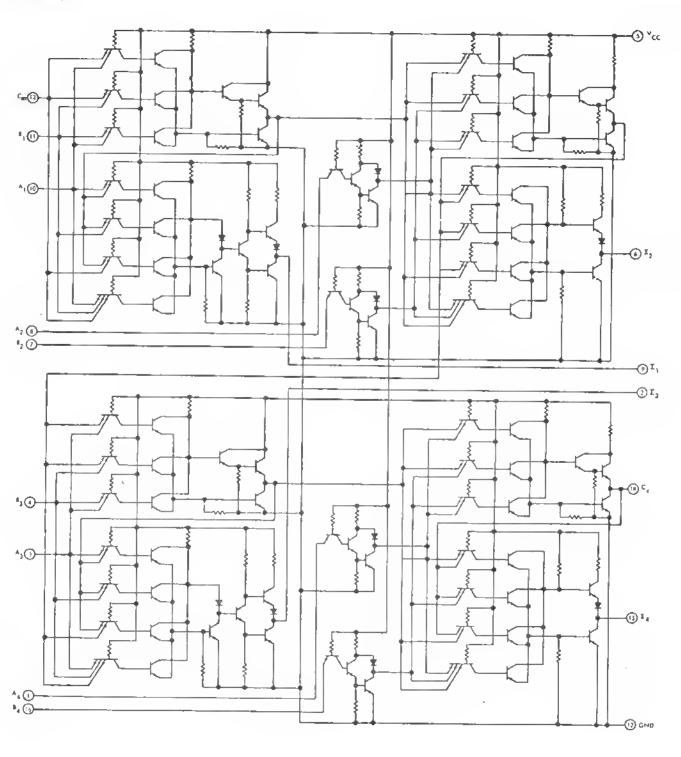
This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) autputs are provided for each bit and the resultant corry (C_s) is abtained from the fourth bit. Designed for medium-ta-high-speed, multiple-bit, perallel-add/serial-carry applications, the circuit utilizes high-speed, high-speed transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "loak-ahead" and carry-cascading circuits. The power dissipation level has been maintained cantiderably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 3 of 10

schematic

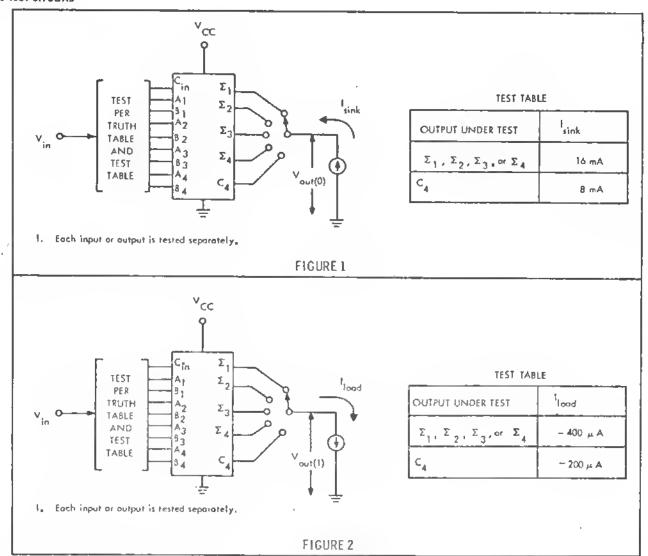


THE FOXBORO COMPANY SYSTEMS DIVISION

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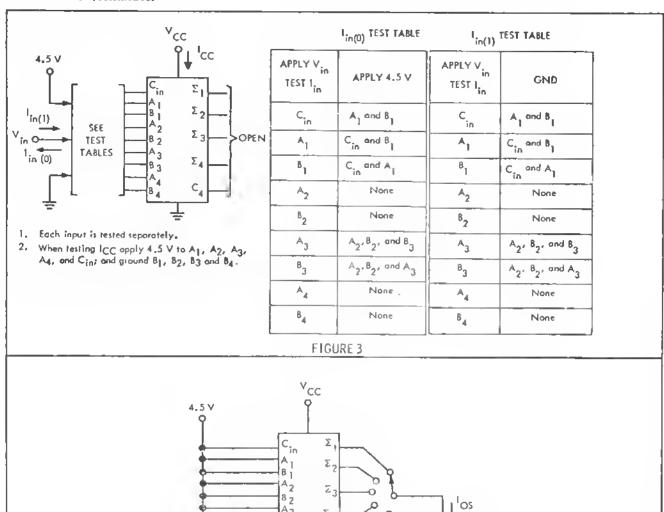
d-c test circuits †



TAirows indicate actual direction of current flow.

THE FOXBORO COMPANY V3003FF

d-c test circuits* (continued)



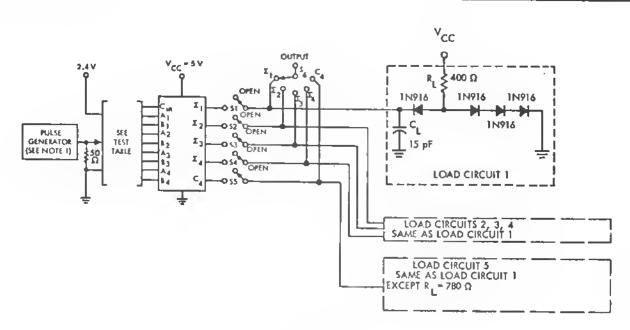
1. Each output is tested separatery.

FIGURE 4

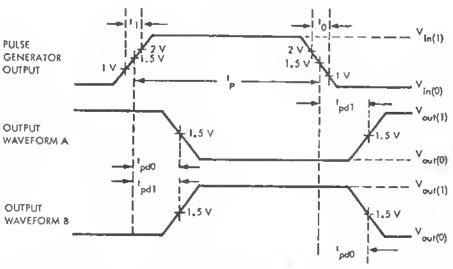
TAirows indicate actual direction of content flow.

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	3>100 00 111 0000 41111 1111		/
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switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: 1. Pulse generator output pulse characteristics: $V_{in(1)} \le 2.4 \text{ V}$, $V_{ln(0)} \le 0.4 \text{ V}$, $t_1 = 8 \text{ to } 15 \text{ ns}$, $t_0 = 3 \text{ to } 5 \text{ ns}$, PRR = 1 MHz, $t_p = 200 \text{ ns}$, and $Z_{out} \approx 50 \Omega$.

- 2. Perform test in accordance with test table. (See sheet 2 of this figure.)
- 3. Each output is tested reparetely.
- 4. Valtage values are with respect to network ground terminal.
- 5. C includes probe and [Ig capacitance.

FIGURE 5 - SWITCHING TIMES (SHEET 1 OF 2)

THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 FF

Sheet 7 of 10

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Rev.

switching characteristics (continued)

TEST TABLE (SEE NOTE 6)

		<u> </u>								
TEST NO.	PARA- METER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (\$6)	APPLY 2.4 V TO	APPLY GND TO	S1	\$2	s3	\$4	\$.5
1	† _{pd1}		Σ		B ₁ , A ₂ ,					
2	P _{pd} 0	Cin	(WAVEFORM A)	^1	and B	CLOSED	OPEN	OPEN	OPEN	OPEN
3	t pd1		Σ							-
4	†pd0	Cin	(WAVEFORM A)	A ₁ and A ₂	B ₁ and B ₂	OPEN	CLOSED	OPEN	OPEN	OPEN
5	t _{pd1}		Σ3	A ₁ , A ₂ ,	B ₁ , B ₂ ,			-		
6	†pd0	C in	(WAVEFORM A)	and A3	end B3	OPEN	OPEN	CLOSED	OPEN	OPEN
7	P _{pd} }		Σ4	A ₁ , A ₂ ,	B ₁ , B ₂ ,					
8	Ppd0	Cin	(WAVEFORM A)	A ₃ , and A ₄	8 ₃ , and 8 ₄	OPEN	OPEN	OPEN	CLOSED	CLOSED
9	[†] pd1		C ₄	A1, A2,	B ₁ , B ₂ ,					
10	pd0	C _{in}	(WAVEFORM 8)	A3, and A ₄	8 ₃ , and 8 ₄	OPEN	OPEN	OPEN	OPEN	CLOSED
11	†pdT		Σ 2		A ₁ , B ₁ ,					
12	¹pd0	A ₂	(WAVEFORM B)	None	B ₂ , and C _{in}	OPEN	CLOSED	OPEN	OPEN	OPEN
13	pdl	B	Σ	NI.	A ₁ , B ₁ ,	OPEN	41045			
14	[†] pd0	B ₂	(WAVEFORM B)	None	A ₂ , and C _{in}	OPEN	CLOSED	OPEN	OPEN	OPEN
15	[†] pd1		Σ 4	None	A ₃ , B ₃ ,	0.0514	0.75			
16	pd0	A ₄	(WAVEFORM B)	None	end B ₄	OPEN	OPEN	OPEN	CLOSED	OPEN
17	[†] pd1	B ₄	Σ 4	None	A ₃ , B ₃ ,	OPEN	OBSN	OPEN	CLOSES	0.000
18	[†] pd0	-4	(WAVEFORM B)	140110	end A ₄	OFEN	OPEN	OPEN	CLOSED	OPEN

NOTE 6: Inputs and outputs not otherwise specified are open.

FIGURE 5 - SWITCHING TIMES (SHEET 2 OF 2)

THE FOXBORO COMPANY V3008FF

SYSTEMS DIVISION

Sheet 8 of 10 /

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absolute maximum ratings over operating	fr	ee-	air	te	mp	era	tur	e i	ran	ge	(ui	nle	SS	oth	erv	vis	еп	ote	d)									
Supply Voltage V _{CC} (See Note 1)	٠	٠		٠	٠	•	٠		٠	٠				٠.			٠				٠	•	٠		٠		7 V	
Input Valtage V_{in} (See Notes 1 and 2).																												
Operating Free-Air Temperature Range Storage Temperature Range	٠		٠	•	•	•	•	٠		٠		٠	•	•		•		٠	•	•	•	•	٠		0 55"	'C N	70°C	
NO1E5: 1. These voltage values are with res 2. Input signals must be positive wit	-										ol.																	
recommended operating conditions																												
Supply Voltage V _{CC}							٠		٠			•		٠	٠	٠	٠	٠	٠					4.	75 V	to .	5.25 V	
Fan-Out From Outputs:																											1 5	
•																												
Σ_1 , Σ_2 , Σ_3 , or Σ_4		٠	•	٠	٠	٠	٠	•	•	•		٠	•	•	•	٠	•	٠	٠	•	٠	٠	٠	•	٠		1 to 10	
electrical characteristics T _A =0°C to 70°C																												

	PARAMETER	TEST •FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
v _{in(1)}	Input voltage required to ensure fagical 1 at any input terminal	I and 2	∨ _{CC} = 4.75 ∨	2			V
V _{in(0)}	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V _{CC} = 4.75 V.			0.8	٧
V _{out(1)}	Logical 1 output valtage	2	V _{CC} = 4.75 ∨	2.4			V
V _{out(0)}	Logical 0 output voltage	1	V _{CC} = 4,75 V			0.4	V
in(0)	Logical O level input current at A ₁ , A ₃ , B ₁ , B ₃ , or C _{1n}	3	V _{CC} = 5.25 V, V _{in} = 0.4 V			-6.4	mA
I _{in(0)}	Logical O level input current at A2, A4, B2, or B4	3	V _{CC} = 5.25 V, V _{in} ≈ 0.4 V			-1.6	mA
l _{in(1)}	Logical 1 level input current at A1. A2. 81. 82. ar Cin	3	$V_{CC} = 5.75 \text{ V}, V_{in} = 2.4 \text{ V}$ $V_{CC}^{\pm} 5.25 \text{ V}, V_{in} = 5.5 \text{ V}$			160	μA mA
1 in(1)	Logical 1 level input current at	3	V _{CC} = 5.25 V, V _{in} = 2,4 V			40	μΑ
in(1)	A2, A4, B2, or 84	,	V _{CC} =5.25 V, V _{in} = 5.5 V			1	mA
los	Shart-circuit output current at Σ_1 , Σ_2 , Σ_3 , or Σ_4 , τ	4	V _{CC} = 5.25 V	-18		-55	mA
los	Shart-circuit output current at C ₄ I	4	V _{CC} = 5.25 V	-18	-	-70	mA
'cc	Supply Current	3	V _{CC} = 5 V, T _A = 25°C		78		mA

[‡] Not more than one output should be shorted at a time.

THE FOXBORO COMPANY V3008FF

SYSTEMS DIVISION

Shoot 9 of 10

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N= 10)

PARAMETER \$	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN TYP	MAX	ואט
†pd1		(001101)	1			34	ns
† _{pd0}	C ^{iu}	1	2			40	กร
r _{pd1}	C		3			38	ns
pd0	Cin	2	4			42	ns
pd)	c		5			50	ns
¹ pd0	C _{in}	3	6			60	ns
f _{pd1}	C		7	_		55	ns
t _{pd} 0	C _{in}	4	8			55	ni
[†] pd1	_	_	9	N = 5	35	43	n:
†pd0	Cin	C ₄	10	N ≈ 5	22	32	ns
[†] pd1	A or B		11 ond 13			40	ns
† _{pd} 0	A ₂ or B ₂	2	12 and 14			35	ns
[†] pd l	A or B		15 ond 17			40	กร
l pd0	A ₄ or B ₄	4	16 and 18			35	ns

Stody is propagation delay time to logical 1 level. to policy is propagation delay time to logical 0 level.

THE FOXBORO COMPANY SYSTEMS DIVISION

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7.	_A	LOCAL RELEASE ECH NO. 1912	1		

1. DESCRIPTION

FIRST USED ON

Circuit, Integrated (Dual In-Line Package)
Decade Counter

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 Sce Sheets 4,5, & 6

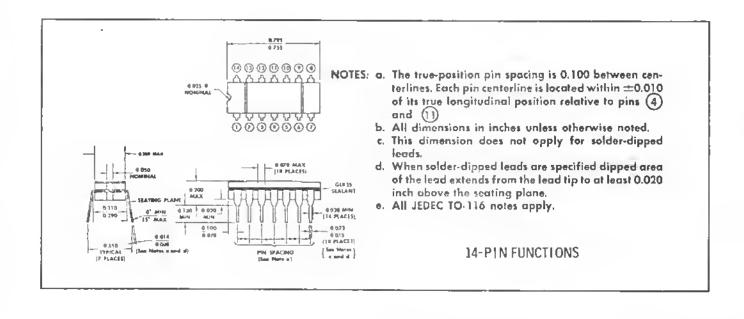
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7490N Sprague Part No. USN7490A National Semiconductor Corp. Part No. OM8530N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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LLV9 OTHERWISE SPECIFIED	WORK AUTH NO.	THE FOXBORO COMPANY
VERDATING SHARPEDNIE WHICH SHAP IN BUCHES WHE ASSELV AFTER PLATIFY THE COLOR OF THE COLOR WHICH SHAP SHAP SHAP SHAP SHAP SHAP SHAP SHA	DARESHOURER CHESCH DOLLAN 7/1/2	TITLE: CIRCUIT, INTEGRATED DUAL IN-LIME PACKAGE TYPE SN74 90N
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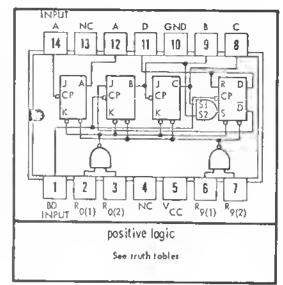
logic

TRUTH TABLES

BCD COUNT SEQUENCE

	(See	<u>Note</u>	1)	
COUNT			PUT	
	D	C	В	A
0	C	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
-4	0	1	0	0
5	0	1	0	1
6	0	1	E	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RES	SET/C	OUNT	(See	Note 2)
R	ESET	NPU1	S	OUTPUT
R _{O(1)}	R ₀₍₂₎	Ř ₉₍₁₎	R ₉₍₂₎	DCBA
1	1	0	Х	0 00 0
1		х	٥	0 00 0
Х	х	1	1	1 001
×	0	х	0	COUNT
0	Х	0	Х	COUNT
0	Х	Х	0	COUNT
_x	0	0	_x	COUNT



NOTES: 1. Output A connected to Input 8D for 8CD count.

2. X Indicates that either a logical 1 or a logical 0 may be present.

description and typical count configurations

The SN7490N is a high-speed, manalithic decade counter consisting of four dual-rank, master-slave flip-flaps internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Goted direct reset lines are provided to inhibit count inputs and return ell outputs to e lagical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be reparated in three independent count modes:

- When used or a binary coded decimel decade counter, the BD input must be externelly connected to the A output. The A Input receives the Incoming count, and a count sequence is obtained in accordance with the BCD count requence truth toble thown above. In addition to a conventional zero reret, input ore provided to reset a BCD 9 count for nine's compliment decimal applications.
- If e symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A Input. The input count is then applied at the BO Input and a divide-by-ten square wave is obtained at output A.
- For operation as a divide-by-two counter and a divide-by-five counter, no externel interconnections are required. Flip-flop
 A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation
 at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset
 simultaneously.

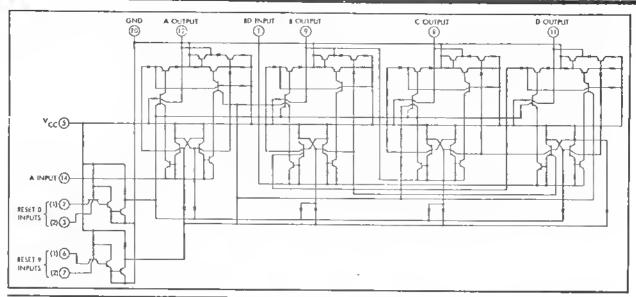
The SN7490N is completely compatible with Series 74 and Series 74 930 TTL, and Series 15 830 DTL logic families. Average power dissipation is 160 mW.

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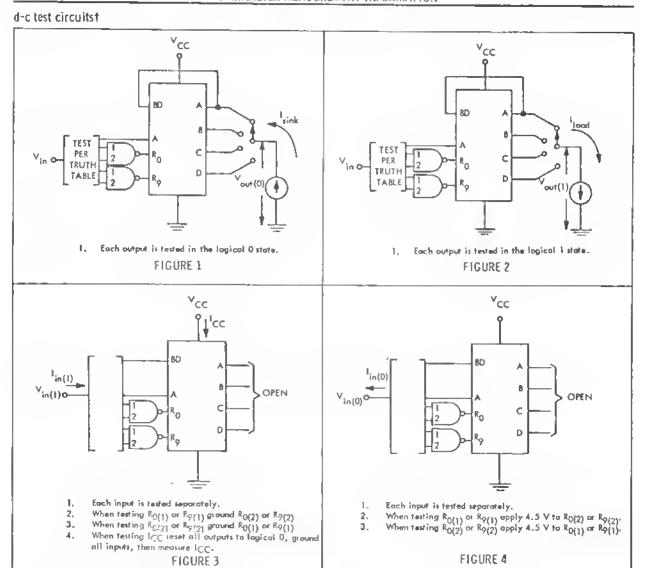
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PARAMETER MEASUREMENT INFORMATION



† Arrows Indicate actual direction of current flow.

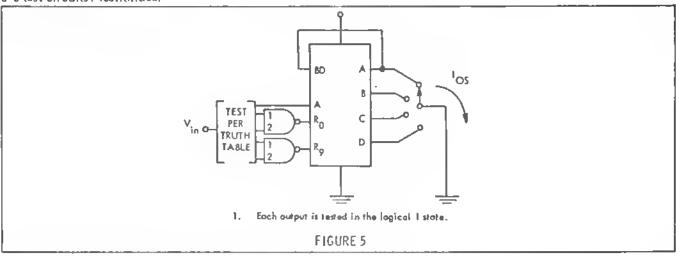
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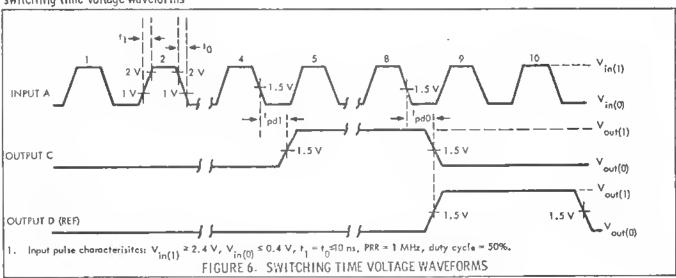
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d-c test circuits† (continued)



† Arrows Indicate actual direction of current flow.

switching time voltage waveforms



THE FOXBORO COMPANY SYSTEMS DIVISION V3008FK

- R.V.

Sheet 5 of 6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V _{CC} (See Note 3)	-	-	-	-				-						-	-	7	V
Supply Voltage V _{CC} (See Note 3) Input Voltage V _{In} (See Notes 3 and 4) .																5.5	V
Operating Free-Air Temperature Range .																0°C to 70°	'C
Storage Temperature Range																	

MOTES: 3. These voltage values are with respect to network ground terminal.

4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V _{CC}													4.7	5 V	to 5.25 V
Fon-Out From Each Output (See Note 5)															1 io 10
Width of Input Count Pulse, tp(In)							٠.								≥ 50 ns
Width of Input Count Pulse, *p(In) Width of Reset Pulse, *p(reset)							÷								≥ 50 ns

NOTE 5: Fan-out from output A to Input BD and to 10 additional Series 74 loads is permitted, electrical characteristics, $T_A = 0^{\circ}C$ to $70^{\circ}C$

	PARAMETER	TEST FIG.	TEST CONDITIONS	MIN	TYP	MAX	UNI
V _{In(1)}	Input voltage required to ensure logical 1 at Inputs A, R ₀ (1), R ₀ (2), R ₉ (1), and R ₉ (2)	1	V _{CC} = 4.75 V	2			٧
V in(1)	Input valtage required to ensure logical 1 at input BD	1	V _{CC} = 4.75 V	2			V
Vin(0)	Input valtage required to ensure logical 0 at inputs A, R ₀ (1), R ₀ (2), R ₉ (1), and R ₉ (2)	2	V _{CC} = 4.75 V			0.6	V
V In(0)	Input valtage required to ensure logical 0 of input 8D	2	V _{CC} = 4.75 V			0.8	V
V_out(1)	Lagical 1 output valtage		V _{CC} = 4.75 V, 1 _{load} = -400 μA	2.4			V
V out(0)	Logical 0 autput valtage	1	V _{CC} = 4.75 V, I _{slnk} = 16 mA			0.4	٧
in(1)	Logical 1 level input current at R ₀₍₁₎ , R ₀₍₂₎ ,	3	V _{CC} = 5.25 V, V _{In} = 2.4 V			40	μΑ
	R9(1)' or R-9(2)		V _{CC} = 5.25 V, V _{In} = 5.5 V			1	mA
in(1)	Logical 1 level input current at input A	3	V _{CC} * 5.25 V, V _{in} = 2.4 V			80	μA
			V _{CC} * 5.25 V, V _{in} = 5.5 V			1	mA
in(1)	Logical 1 level input current at input 80	3	V _{CC} = 5.25 V, V _{in} = 2.4 V			160	μA
			V _{CC} = 5.25 V, V _{In} = 5.5 V			1	mA
in(0)	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(3)}$, ar $R_{9(2)}$	4	V _{CC} = 5.25 V, V _{In} = 0.4 V			-1.6	mA
In(0)	Logical O level input current at input A	4	V _{CC} = 5.25 V, V _{In} = 0.4 V			-3.2	mA
ln (0)	Logical 0 level input corrent of input BD	4	V _{CC} = 5.25 V, V _{In} = 0.4 V			-6.4	mA
los	Short-circuit autput current?	5	V _{CC} = 5.25 V, V _{out} = 0 V	-18		-57	mА
l _{cc}	Supply Current	3	V _{CC} = 5 V , T _A = 25°C		32		mA

Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$, N = 10

	PARAMETER	TEST FIG.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f max	Maximum frequency of input count pulses			10	16		MHz
[†] pd1	Propagation delay time to logical 1 level from Input count pulse to output C	6			60	100	ns
[†] pd0	Propagation delay time to logical O level from input count pulse to output C	6			60	100	ns.

THE FOXBORO COMPANY SYSTEMS DIVISION

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FIRST USED ON		REVISIONS			
	LTR	DESCRIPTION	OR	DATE	APPROVEO
	Α	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
8-Sit Shift Register

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet \$.5,6 & 7
- 4. MANUFACTURER'S NAME AND PART NO.

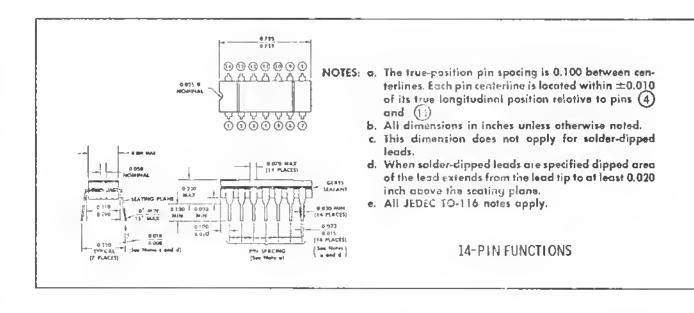
Texas Instrument, Part No. SN7491AN Sprague Part No. USN7491A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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01.008: ±1/84 1:ALS: ±.005 1:5 : ±1/2°	B Wally	3/4/	1	-LING PACKAGE YPE SN7+91AN	
ATERIAL!	T. Dinta	3/24/20	SIZE SYMBOL DR	AWING NO.	REV
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THE FOXBORO COMPANY SYSTEMS DIVISION

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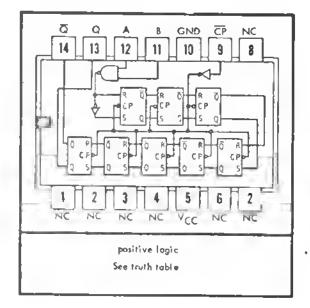
togic

TRUTH TABLE

ŀ	n	† _{n+8}
A	В	Q
0	0	0
0	1	0
1	0	0
1	1	-

NOTES: 1. $t_n = hit$ (Ime before clock pulse.

2. $t_{n+8} = 611$ time ofter 8 clock pulses,



description

The SN7491AN is a monolithic serial—aut, 8-bit shift register utilizing stansinter-transistor logic (TTL) circuits in the familiar high-speed Series 54 configuration. The shift register, composed of eight 8-5 moster-slave flip-flops, includes input gating and a clack driver. The register is capable of storing and stansferring data at clock rates up to 18 MHz while maintaining a sypical noise-immunity level of 1 volt. Power dissipation is typically 175 millimatts, and full fan-out of f0 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B and \overline{CP}) appear as only one TTL input load.

The clock pulse inverter/driver causes the SN7491AN to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with the SN7470 J-K flip-flop and the SN7474 dual D-type flip-flop.

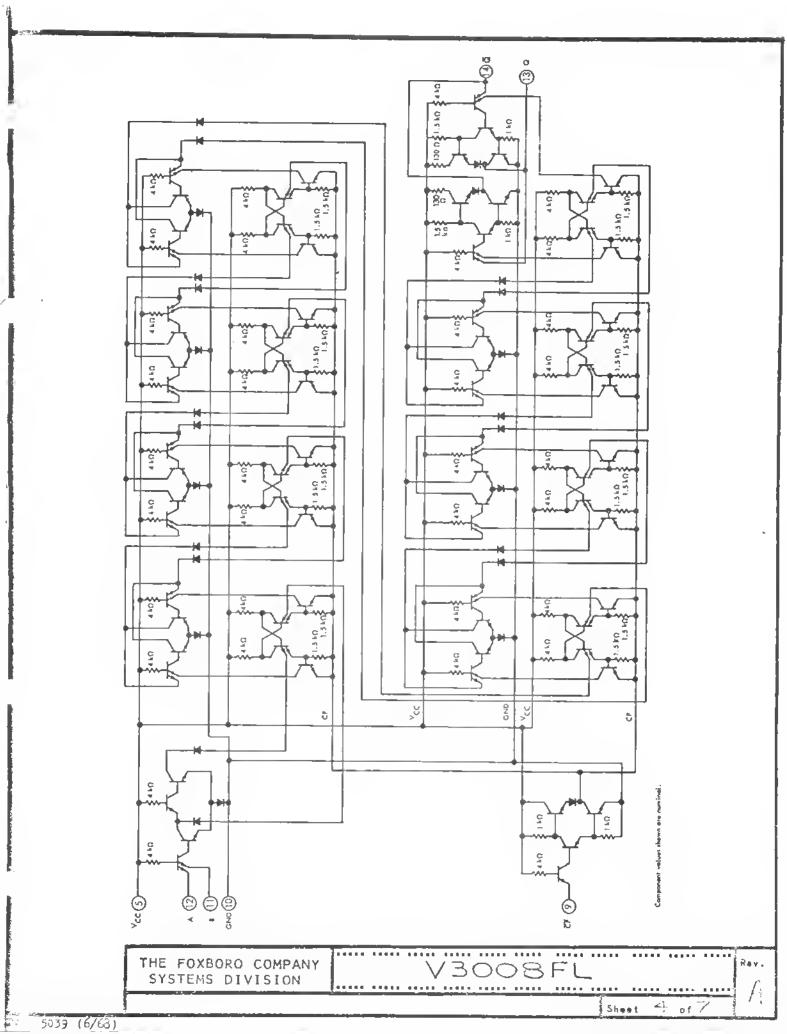
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V3008 FL

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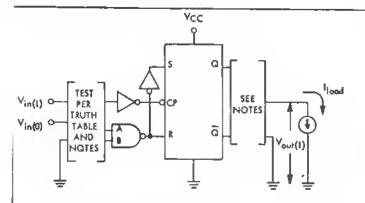
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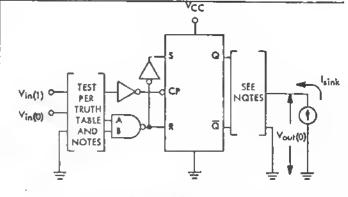


PARAMETER MEASUREMENT INFORMATION

d-c test circuits §



- 1. Each output is tested separately.
- 2. When testing $V_{out}(l)$ and $l_{load},$ ground all inputs and the unused output, then measure parameters specified .



1. Each output is tested separately.

lin(t)

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NOTES

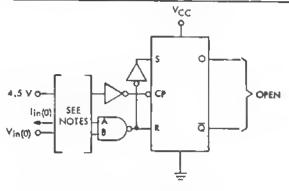
 When testing V_{OUT}(0) and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified. FIGURE 2

V_CC

₫

OPEN

FIGURE I



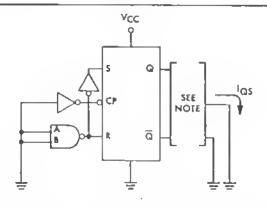
- 1. When testing input Alopply 4.5 V to input 8,
- 2. When testing Input 8 apply 4.5 V to input A.



1. When testing input A ground input B.

2. When testing input 8 ground input A.

FIGURE 3



1. Ground the unused output then measure parameter specified.

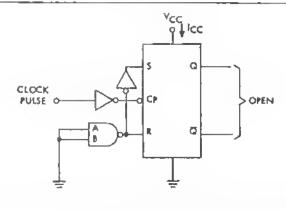


FIGURE 4

MEASURE ICC

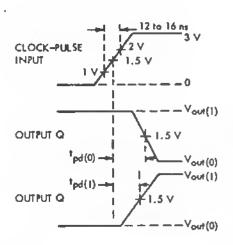
FIGURE 6

FIGURE 5

I Arrows Indicate actual direction of current flow.

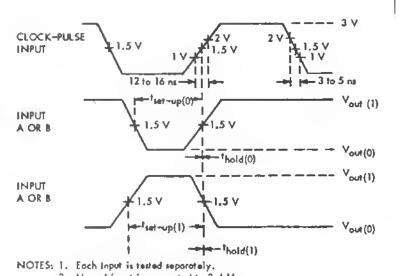
THE FOXBORO COMPANY SYSTEMS DIVISION

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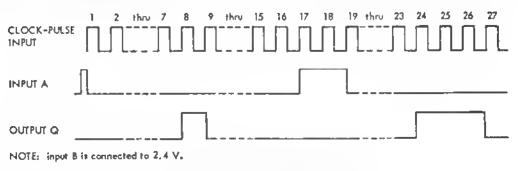
NOTE: The clock-pulse has the following characteristics: PRR = 1 MHz and duty cycle = 50%.

PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS



 Unused input is connected to 2.4 V
 The clock-pulse has the following characteristics: PRR = 1 MHz and duty cycle = 50%.

SWITCHING TIMES VOLTAGE WAVEFORMS



TYPICAL INPUT/OUTPUT WAVEFORMS
FIGURE 7 — SWITCHING TIMES

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SYSTEMS DIVISION

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Sheet 6 of 7

absolute maximum ratings over operating free-air temperature range

Supply Voltage VCC (See Note 3)																				7 V	ï
Input Voltage Vin (See Notes 3 and 4)									-			Ī	Ť	٠	•	•	•	•	٠,	. 5 V	ï
Operating Free-Air Temperature Range						_	Ĭ		-	Ť	•	•	•	•	•	•	•	0.0	100	70°C	
Storage Temperature Range						Ī	-					:	•	•			-59	500	io 1	75°C	ć

NOTES: 3. Voltage values are with respect to network ground terminal.

4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage VCC	٠	٠	•	•	٠	٠	٠	-	٠										4	.75	VI.	o 5.2	25 1	V
Fon-Out From Outputs		٠			-	•						-										I to	. 1	0

electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0 to 70°C

	PARAMETER	MIN	TYP	MAX	UNIT
V _{in(1)}	Logical 1 input valtage	2		-	٧
V _{in(0)}	Logical O Input valtage			0.8	V
Vout(1)	Logical I output voltage (N = 10)	2.4			
V _{out (0)}	Lagical 0 output voltage (N = 10)			0.4	V
lin(1)	Logical 1 level input current at any input			40	μA
in(0)	Logical O level input current at any input			-1.6	mA
los	Short-circuit output current	-18		-55	mA
^l cc	Supply current (TA = 25°C)		35	70	mA

switching times, V_{CC} = 5 V, T_A = 25°C (See Figures 1 and 2)

	PARAMETER	MIN	TYP	MAX	UNII
f max	Maximum shift frequency	10	18		MHz
[†] p(clock)	Minimum clock pulse width		18	25	na
fset~up(0)	Minimum logical 0 level set-up time required at A or 8 inputs		12	25	n#
fset-up(1)	Minimum logical 1 level set-up time required at A or 8 inputs		15	25	ns.
hold(0)	Logical O level hold time required at A or 8 input		-15	0	ns
thold(1)	Logical 1 level hold time required at A and B inputs		-12	0	ns
tpd(1)	Propagation delay time to logical 1 level (clock-to-output)		24	40	ns
¹ pd(0)	Propagation delay time to logical Ollevel (clack-to-output)		27	40	ns.

[†] When the unused input is at logical 1.

THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 FL

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Sheet 7 of 7

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1. DESCRIPTION

FIRST USED ON

Circuit, Integrated (Dual In-Line Package) Divide by 12 Counter

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 4.5, & 6

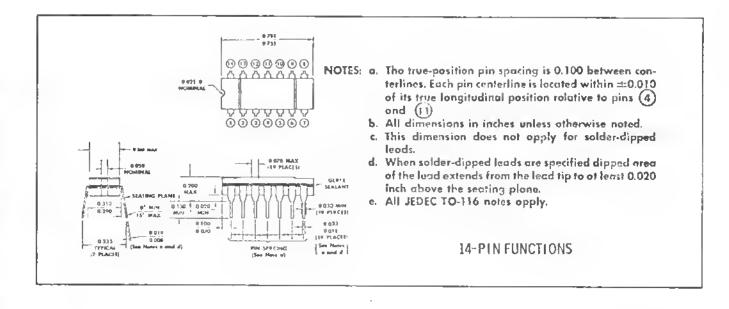
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7492N Sprague Part No. USN7492N National Semiconductor Part No. DM8532N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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THE FOXBORO COMPANY SYSTEMS DIVISION

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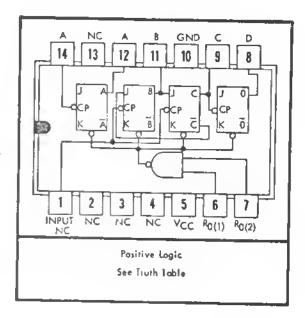
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TRUTH TABLE (Sie Notes 1 and 2)

COUNT		ΟU	TPUT	
	D	C	В	Α
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	Ι	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES: 1. Output A connected to Input 8

2. To reset all outputs to logical 0 both R_{O(1)} and R_{O(2)} inputs must be at logical 1.



description

The SN7492N is a high-speed monolithic 4-bit binary counter consisting of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

- When used as a divide-by-twelve counter, output A must be externally connected to input BC. The Input count pulses
 are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in
 the truth table above.
- When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously frequency divisions
 of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available If the reset function coincides with teset of the divide-by-six counter.

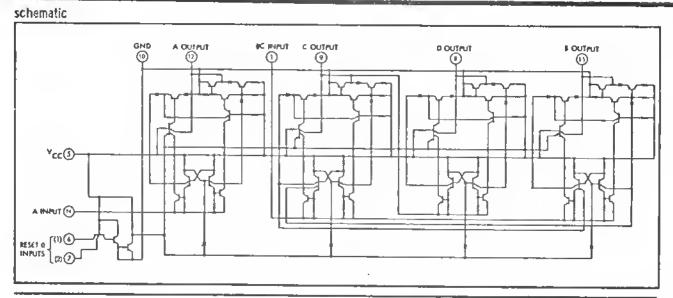
The SN7492N Is completely compatible with Series 74 and 74 930 TTL, and Series 15 830 OTL logic families. Average power dislipation is 155 mW.

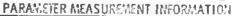
THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 FM

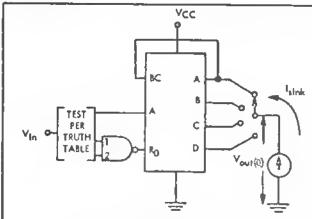
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Sheet 3 of 6



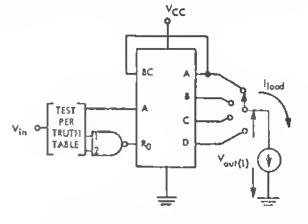






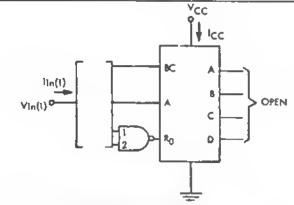
1. Each output is tested in the logical O state.

FIGURE 1



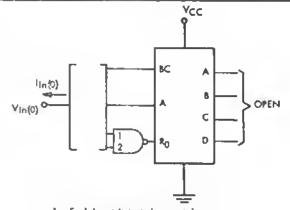
1. Each output is tested in the logical Latate.

FIGURE 2



- 1. Each Input Is tested separately,

- When fasting Ro(1) ground Ro(7).
 When testing Ro(2) ground Ro(7).
 When testing ICC reset all outputs to logical 0, ground att inputs, then measure ICC. FIGURE 3



- 1. Each linear is tested separately. 2. When fasting $R_0(z)$ apply 4.5 V to $R_0(z)$. 3. When testing $R_0(z)$ apply 4.5 V to $R_0(z)$.

FIGURE 4

†Arrows Indicate actual direction of current flow,

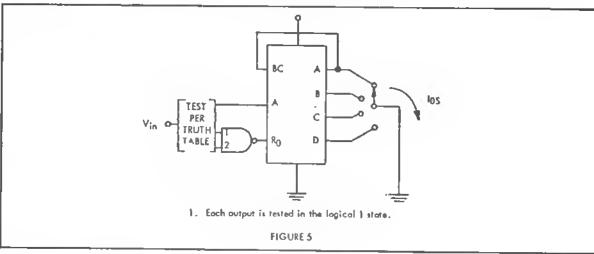
THE FOXBORO COMPANY SYSTEMS DIVISION

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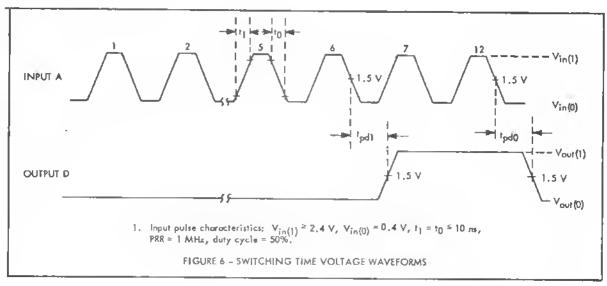


d-c test circuits† (continued)



farrows indicate actual direction of current flow

switching time voltage waveforms



THE FOXBORO COMPANY SYSTEMS DIVISION

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Rev.

Sheet 5 of G

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

7 V

5.5 V Storage Temperature Range

NOTES: 3. These voltage values are with respect to network ground terminal

4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V _{CC}	٠.							٠.														4.	75	V to	5.2	25	v
Fan-Out From Each Output (Se	e No	te i	5)									 		 											1 6	~ . 1	'n
Width of Input Count Pulse, tp(in)											 			Ť	Ĭ		•	٠	•	•		•		≥ 5		
Width of Reset Pulse, tp(reset)			٠				_				-				٠	•		• •	•		•	•				u r	13

NOTES: 5. Fan-out from output A to input BC and to 10 additional Series 74 loads is permitted.

electrical characteristics, TA = 0°C to 70°C

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vin(1)	Input voltage required to ensure logical 1 of inputs A, RO(1), and RO(2)	1	V _{CC} = 4.75 V	2			V
Vin(1)	Input voltage required to ensure logical Lat input BC	1	V _{CC} = 4.75 V	2.2			٧
Vin(0)	Input voltage required to ensure logical 0 at inputs A, RO(1), and RO(2)	2	V _{GC} = 4.75 V			0.8	٧
Vin(0)	Input voltage required to ensure logical 0 at input 8C	2	V _{CC} = 4.75 V			0.6	٧
Vout(1)	Logical I output valrage	2	V _{CC} = 4.75 V, I _{land} = -400 µA	2,4			
Vout (0)	Logical O output valtage	1	V _{CC} = 4.75 V, i _{sink} = 16 mA	-		0.4	V
ta(1)	Logical I level input current at	3	V _{CC} = 5.25 V, V _{tn} = 2.4 V			40	μA
	RO(1) or RO(2) inputs		V _{CC} = 5.25 V, V _{in} = 5.5 V			1	mA
in(1)	Logical 1 level input current at input A	3	V _{CC} = 5.25 V, V _{IB} = 2.4 V V _{CC} = 5.25 V, V _{IB} = 5.5 V			80	μA
- 413	<u> </u>		, CC 2:22 4, 4 ^{iu} 2:24	_			mA
in(1)	Logical 1 level Input current at Input BC	3	V _{CC} = 5.25 V, V _{tn} = 2.4 V V _{CC} > 5.25 V, V _{tn} = 5.5 V			160	μA
in(0)	Logical O level input current of RO(1) or RO(2) inputs	4	V _{CC} = 5.25 V, V _{in} = 0.4 V			-1.6	mA
in(0)	Logical O level input current of input A	4	V _{CC} = 5,25 V, V _{in} = 0.4 V			-3.2	mΑ
in(0)	Logical D level input current at input BC	4	V _{CC} = 5.25 V, V _{in} = 0.4 V			-6.4	mÅ
20	Short-circuit output current †	5	V _{CC} = 5.25 V, V _{out} = 0	-18		-57	mΑ
CC	Supply Current	3	V _{CC} = 5 V , T _A = 25°C		31		mA

†Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$, N = 10

	PARAN'ETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Maximum frequency of Input count pulses			10	18		MHz
[†] pd1	Propagation delay time to logical 1 level from input count pulse to output D	6			60	100	ns
t _{pd0}	Propagation delay time to logical 0 level from input count Pulse to output D	6			60	100	ns

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A	LOCAL RELEASE EGN NO. 1914			

1. DESCRIPTION

FIRST USED ON

Circuit, Integrated (Dual In-Line Package)
4-Bit Binary Counter

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 4,5 & 6

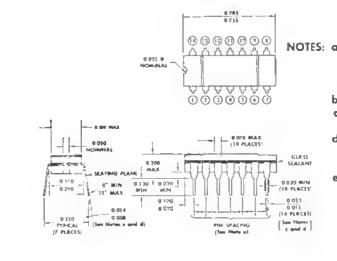
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7493N Sprague Part No. USN7493A National Semiconductor Corp. Part No. BM8533N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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DE LA CALL CU DE LA	CHESTER (1) 20 Step) 1/4/	CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN74 93N
INISH:	REL ASLU	SIZE SYMBOL DRAWING NO. REV
- 5053A (4/67)	LOCAL RELEASE	SCALE: NONE SHEET LOFG



NOTES: a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lend extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

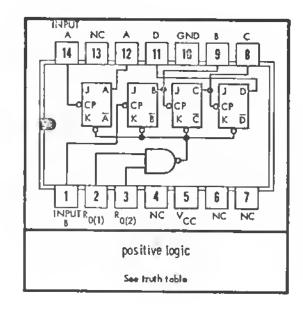
THE FOXBORO COMPANY SYSTEMS DIVISION

Rav.

logic

TRUTH TABLE (See Notes 1 and 2)

		ÓUI	PUT	
COUNT	D	c	В	*
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1_
4	0	1	o	0
5	0	1.	0	i
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	i	0
11	1	0	-	1
12	1	1	0	0
13	1	1	0	1
14	1	i	1	0
15	1	: I	1	ī



NOTES: 1. Output A connected to Input B.

2. To reset all outputs to logical 0 both $R_{O(1)}$ and $R_{O(2)}$ inputs must be at logical 1.

description.

The SN7493N is a high-speed, manufille 4-bit binary counter consisting of four master-slave filip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A goted direct reset line is provided which inhibits the count inputs and simultaneously returns the four filip-flop autputs to a logical 0. As the autput from filip-flop A is not internally connected to the succeeding filip-flops, the counter may be operated in two independent modes:

- When used as a 4-bit ripple-through counter, output A must be externally connected to input 8. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and 0 outputs as shown in the truth table above.
- When used as a 3-bit ripple-through counter, the input count pulses are applied to input 8. Simultaneous frequency divisions of 2,
 4, and 8 are available at the 8, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

The SN7493N is completely compatible with Series 74 and Series 74 930 TTL, and Series 15 830 DTL logic families. Average power dissipation is 32 mW per flip-flop (128 mW total).

THE FOXBORO COMPANY SYSTEMS DIVISION

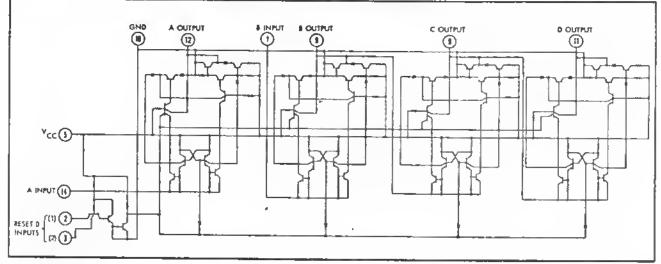
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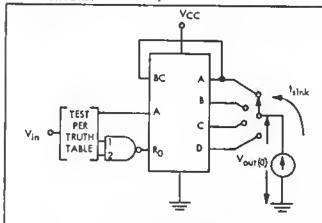
| Sheet - of C

PARAMETER MEASUREMENT INFORMATION

schematic

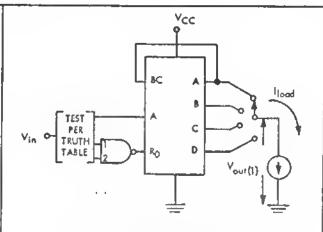


d-c test circuits†



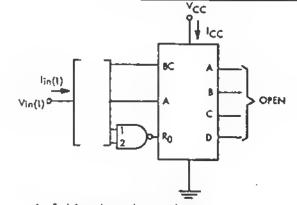
1. Each output is tested in the logical O state.

FIGURE 1



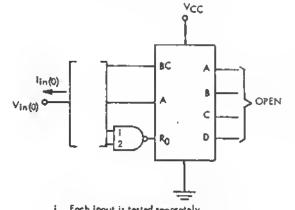
1. Each output Is tested in the logical 1 state.

FIGURE 2



- 1. Each input is tested separately.
- When testing Ro(1) ground Ro(2).
- 3. When testing RO(2) ground RO(1)
 4. When testing ICC all inputs and outputs are open.

FIGURE 3



- Each Input is tested separately.
 When testing RO(t) apply 4.5 V to RO(2).
- 3. When testing RO(2) apply 4.5 V to RO(1).

FIGURE 4

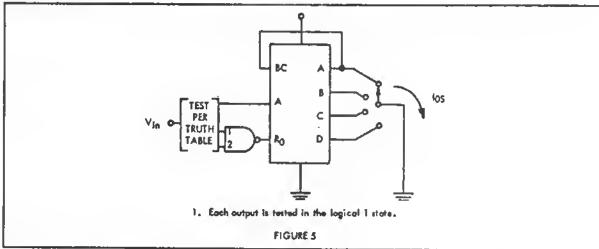
†Arrows indicate actual direction of current flow.

THE FOXBORO COMPANY SYSTEMS DIVISION

of V Sheet

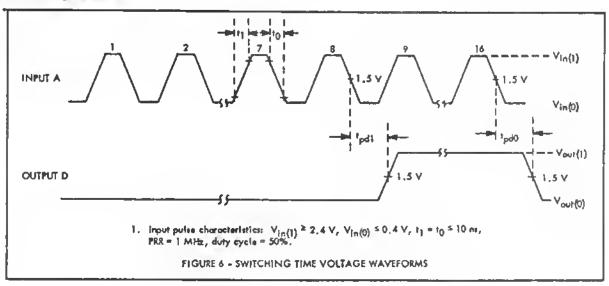
PARAMETER MEASUREMENT INFORMATION

d-c test circuitst (continued)



forrows indicate actual direction of current flow

switching time voltage waveforms



THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 5 of 6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V _{CC} (See Note 3)																	7 V	,
Input Voltage V _{In} (See Notes 3 and 4)		٠	٠	٠													5.5 V	/
Operating Free-Air Temperature Range	٠			٠											0	*C 1	6 70°C	
Storage Temperature Range														-	55*	Cin	125*0	

NOTES: 3. These voltage values are with respect to network ground terminal.

4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V _{CC}			·											4,7	/5 V t	o 5.25 V
Fon-Out From Ench Output (See Note 5)																1 to 10
Width of Input Count Pulce, tofin)																≥ 50 ns
Width of Reset Pulse, t p(reset)				÷						į.						≥ 50 ns

NOTES: 5. Fam-out from output A to Input B and to 10 additional Series 74 loads is permitted.

electrical characteristics, T_A - 0°C to 70°C

	PARAMETER	TEST FIG.	TEST CONDITIONS	MIN	TYP	мах	וואט
Y _{in(1)}	input voltage required to ensure logical 1 at inputs A, $R_0(1)^r$ and $R_0(2)$	1	V _{CC} = 4.75 V	2			٧
Υ _{ΙΛ(1)}	input voltage required to ensure logical E at input B	1	V _{CC} = 4.75 V	2			V
V _{In(0)}	Input voltage required to ensure logical 0 of inputs A, $R_{O(1)}$, and $R_{O(2)}$	2	V _{CC} = 4.75 V			0.8	٧
V _{in(0)}	Input voltage required to ensure logical 0 at input B	2	V _{CC} = 4.75 V	 		8.0	٧
V _{ov1(1)}	Lagical 1 output valtage	2	V _{CC} = 4,75 V, I _{load} = ~400 μA	2.4			V
V _{ovi} (n)	Logical 0 output voltage	1	V _{CC} = 4.75 V, I _{sink} = 16 mA	 	-	0,4	V
l _{In(1)}	Logical 1 level input current of R _{O(1)} or R _{O(2)} inputs	3	V _{CC} = 5,25 V, V _{in} = 2,4 V V _{CC} = 5,25 V, V _{in} = 5,5 V			40	μΛ
I _{In(1)}	Logical 1 level input current at A or 8 inputs	3	VCC = 5. 5 V, V, = 2.4 V VCC = 5.5 V, V _{id} = 5.5 V			६३	65A 450
in(°)	Logical 0 isvel input current of R _{O(1)} or R _{O(2)} inputs	4	V _{CC} = 5.25 V, V ₁₀ = 0.4 V			-1.6	mA
i _{n (0)}	Logical C level Input current of A or 8 Inputs	4	V _{CC} = 5.25 V, V _{in} = 0.4 V	_		-3.2	mA
CI	Short-circuit output exerent T	5	V _{CC} = 5.25 V, V _{out} = 0	-18		-57	mA
t _{CC}	Supply current	3	V _{CC} = 5 V		32		mA

[†] Not more than one autput should be shorted at a time

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST FIG.	TEST CONDITIONS	MIN	TYP	MAX	זואט
f max	Maximum frequency of Input count pulses			10	10		MHz
t _p (1	Proposition delay time to logical 1 level from Input count pulse to output D	6			75	135	nı
[†] pd0	Proposetion datay time to logical 0 level from input count pulse to output D	6	.,		75	135	na

THE FOXBORO COMPANY B V3005 FN
SYSTEMS DIVISION B V3005 FN
Sheet G of G

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ISHEET I OF

1. DESCRIPTION

FIRST USE

Circuit, Integrated (Dual In-Line Package)
4-Bit Shift Register

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 2
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 5
- 4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN74 94N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT 1. YES OTHERWISE SPECIFIED WORK AUTH NO. THE FOXBORO COMPANY STRUCK SHANE & SKAND EDETP FOXBORO, MASSACHUSETTS, U.S.A. DRASTA Walker DETE. LEASIONS ARE IN INCHES . Uthis apply apter plating TITLE: CIRCUIT, INTEGRATED A 028 CH STIONS: ± 1/64 DUAL IN-LIBE PACKAGE - 1/2° 29/ TYPE SN74 94N 1 1 U M . 2 SATERIALI SIZE SYMBOL & DRAWING NO. REV SEAL P

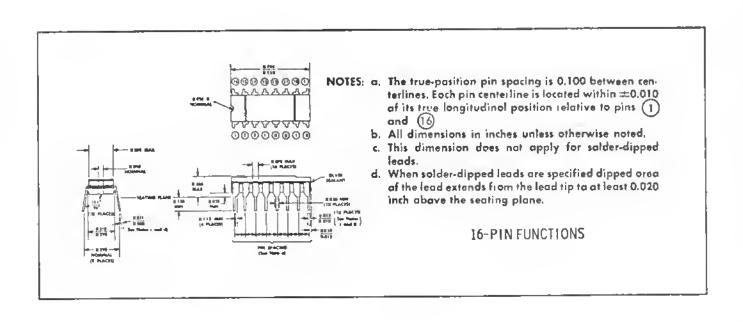
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THE FOXBORO COMPANY SYSTEMS DIVISION

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Sheet 2 of 5

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description

This monalithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar. Series. 74 configuration, is composed of four R-S moster-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versative register which performs right-shift aperations at a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an arbit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 valtage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to present 1 If preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flaps are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flap prior to the rising edge of the clock input wave-

form. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input and either preset 1 or preset 2 must be at a logical 0 when clacking occurs.

This register is completely compatible for uso with TTL and OTE togic circuits and when used with other TTL circuits typical one volt naise margins are maintained. Typical overage power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 40 nanaseconds.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V _{CC} (See Note 1)	٠	٠	٠	٠	٠		٠	٠	٠	٠	٠	٠	٠		٠			٠			٠		٠			7 '	V
Input Voltage V _{In} (See Notes 1 and 2)	٠	٠	٠	٠		٠	٠	٠	٠	٠	٠	٠	٠			٠	٠	٠	٠		٠			٠		5.5	٧
Operating Free-Air Temperature Range	٠	٠	٠		٠	٠	٠	٠	٠	٠	٠	٠		٠	•	٠	٠		٠	٠	•	٠			0°C	to 70°0	C
Storage Temperature Ronge																	٠						٠	-	55°C 1	o 150°	C

NOTES: 1. These valtage values are with respect to network ground terminal.

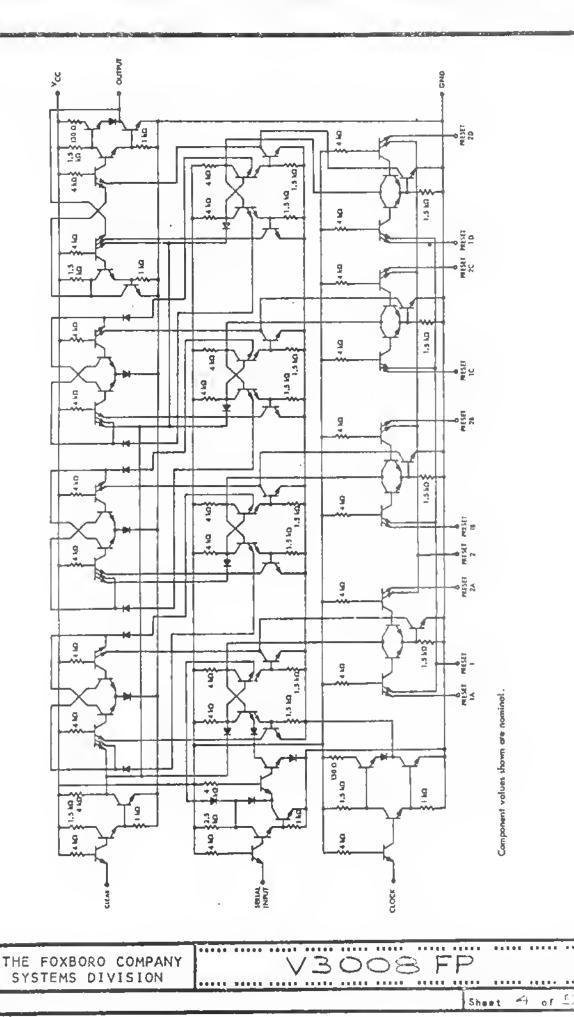
2. Input signals must be zero or positive with respect to network ground terminal.

THE FOXBORO COMPANY SYSTEMS DIVISION

V3008 FP

Rev

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recommended operating conditions

										MIN	TYP	MAX	UNIT	
Supply Voltage V _{CC} (See Note 1)				٠.						4.75	5	5.25	٧	Ī
Fon-Out from Output												10		-
Width of Clock Pulse, tp(clock)	٠							٠		35			D\$	
Width of Clear Pulse, tp(clear)										30			n.	
Width of Preset Pulse, tp(preset)										30			nı.	
Serial Input Setup Time: t setup(1)									-	35			ns	Ì
setup(0)										25			ns.	
Serial Input Hold Time, Phold										0				

NOTE 1: These voltage values are with respect to network ground terminal.

electrical characteristics (over operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIM	TYP	MAX	TINU
V _{in(1)}	Input valtage required to ensure logical 1 at any input terminal	V _{CC} = MIN	2			٧
V _{In} (0)	Input voltage required to ensure lagical 0 at any input terminal	V _{CC} = MIN			0.8	V
V _{out} (1)	Logical 1 output voltage	V _{CC} = MIN, 1 _{lood} = -400 μA	2.4	3.5		٧
V _{out} (0)	Logical 0 output voltage	V _{CC} = MIN, I _{sink} = 16 mA		0.22	0.4	V
l. ,,,	Logical 1 level input current at	V _{CC} = MAX, V _{to} = 2.4 V			40	μА
in(1)	any input except Preset 1 and Preset 2	V _{CC} = MAX, V _{in} = 5.5 V			I	mA
l	Logical Lievel input current at	V _{CC} = MAX, V _{in} = 2.4 V			160	μА
ln(1)	Preset 1 and Preset 2	V _{CC} = MAX, V _{In} = 5.5 V			1	mA
l _{In(0)}	Logical Ofevel input current at any input except Preset I and Preset 2	V _{CC} = MAX, V _{In} = 0.4 ∨			-1.6	mA
I _{In(0)}	Logical Olevel input current at Preset 1 and Preset 2	V _{CC} = MAX, V _{in} = 0.4 V			-6.4	mA
os	Short-circuit output current9	V _{CC} = MAX, V _{aut} = 0	-18		-57	mА
cc	Supply current	V _{CC} = MAX		35‡	57	mΑ

For conditions shown as MIN or MAX, use the appropriate value specified under recommended aperating conditions. These typical values are at V_{CC} = 5 V, T_A = 25 °C. Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}	Maximum clock frequency	C _L = 15 pF, R _L = 400 Ω	10			MHz
[†] pd1	Propagation delay time to logical 1 level from clock to autput	C _L = 15 pF, R _L = 400 Ω		25	40	TH.
† _{pd0}	Propagation delay time to logical O level from cl ock to output	C _L = 15 pF, R _L = 400 Ω		25	40	ns
†pd1	Propagation delay time to logical 1 level from Preset to autput	C _L = 15 pF, R _L = 400 Ω			35	ns
[†] pd0	Propagation delay time to logical 0 level from clear to output	C _L = 15 pF, R _L = 400 Ω			40	Už

THE FOXBORO COMPANY SYSTEMS DIVISION

FIRST USED ON		REVISIONS			
	LTR	OESCRIPTION	OR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1917			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
4-3it Shift Register Right Shift - Left Shift

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 5,6,7,8 & 9

4. MANUFACTURER'S NAME AND PART NO.

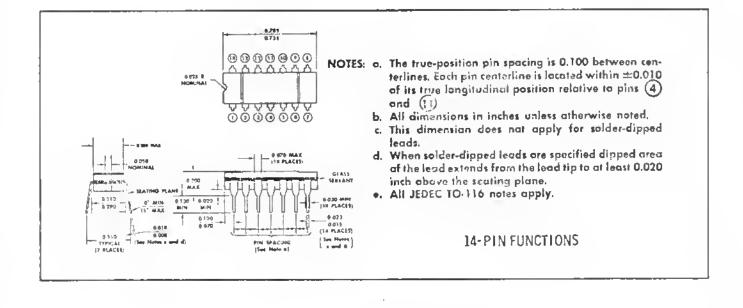
Texas Instrument, Part No. SN7495N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

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THE FOXBORO COMPANY SYSTEMS OLVISION

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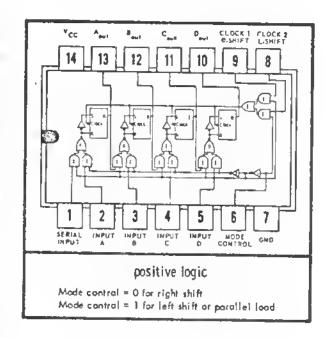
This monolithic shift register, utilizing transistar-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S moster-slave flip-flops, faut AND-OR-INVERT gater, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift aperations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out staroge register with gate (mode) control.

When a logical Olevel is applied to the mode control input, the number 1 AND gates are enabled and the number 2 AND gates are inhibited. In this mode the autput of each flipflip is caupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clack 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a logical 1 level is applied to the mode control input, the number I AND gates are inhibited (decoupling the autputs from the succeeding R-S inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by cannecting the autput of each flip-flap to the parallel input of the previous flip-flap (Daut to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used far the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clack 2. Information must be present at the R-S inputs of the master-slave flip-flaps prior to clocking.

The shift register is completely compatible with Series 74 and Series 15 830 DTL lagic families. Average power dissipation is typically 250 milliwatts.



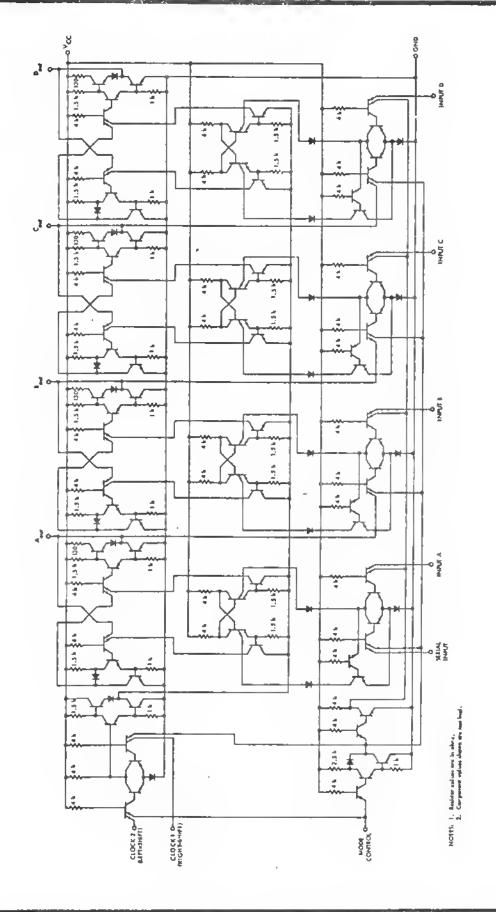
THE FOXBORO COMPANY SYSTEMS DIVISION

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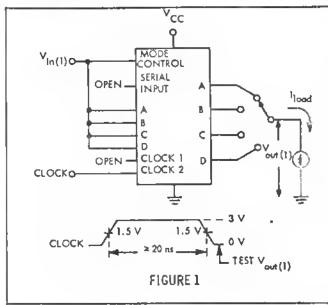
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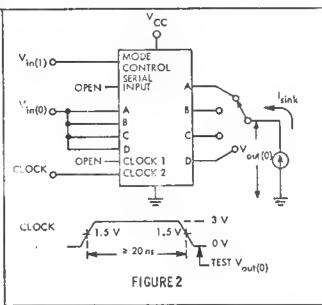
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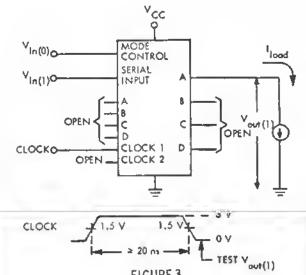
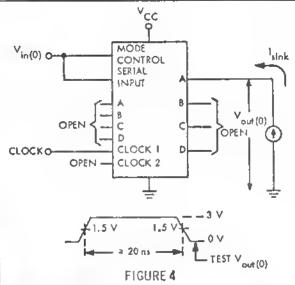
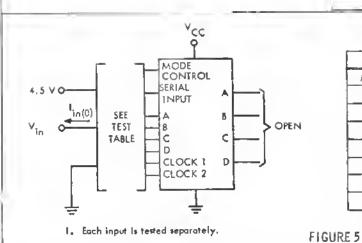


FIGURE 3



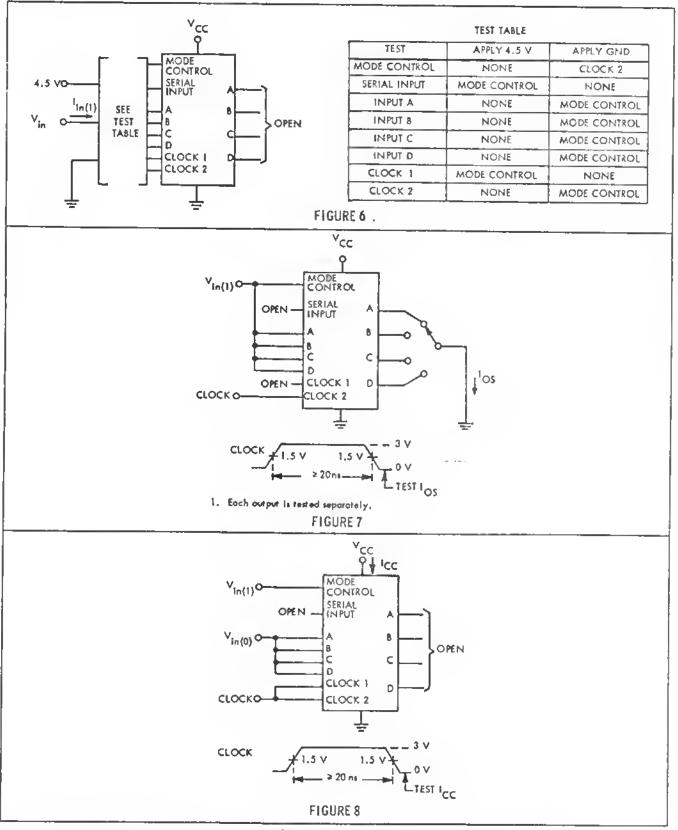


	IEST TWOLE	
TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INIPUT	NONE	MODE CONTROL
INFUT A	MODE CONTROL	NONE
INPUT 8	MODE CONTROL	NONE
INFUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

†Arrows indicate actual direction of current flow.

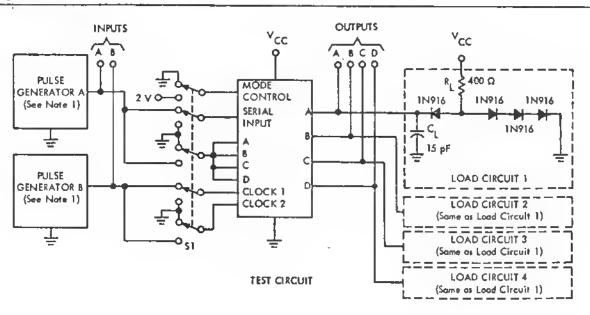
THE FOXBORO COMPANY SYSTEMS DIVISION

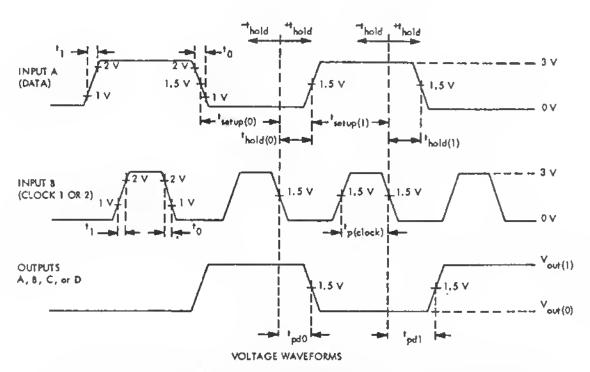
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†Arrows indicate actual direction of current flow.

THE FOXBORO COMPANY SYSTEMS OLVISION V3008 FR





NOTES: 1. The pulse generators have the following characteristics: $V_{gen} = 3 \text{ V, } t_1 = 12 \text{ to 16 ns, } t_0 = 3 \text{ to 5 ns, and}$ $Z_{out} \approx 50 \,\Omega$. For pulse generator A: $t_p \ge 20 \text{ ns and PRR} = 500 \text{ kHz}$. For pulse generator B: $t_p \ge 15 \text{ ns and}$ PRR = 1 MHz. When testing f_{max} vary PRR,

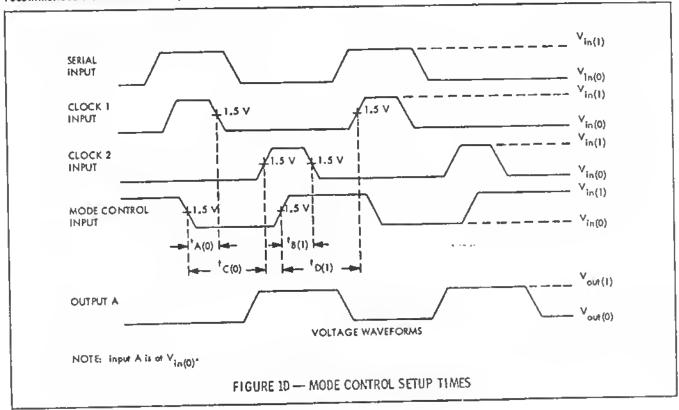
2. Voltage values are with respect to network ground terminal.

3. C, includes probe and Jig capacitance.

FIGURE 9 - SWITCHING TIMES

THE FOXBORO COMPANY SYSTEMS DIVISION V3008 FR

recommended mode control setup times



THE FOXBORO COMPANY SYSTEMS DIVISION

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Rev.

Sheet 😂 of 🗓

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V _{CC} (Sex Note 1)														7	٧
Input Valtage V _{In} (See Notes 1 and 2)								÷						5.5	٧
Operating Free-Air Temperature Range												0	/*C1	o 70°	C
Storoge Temperature Range											-	55"	Cit	150	C

recommended operating conditions

								MIN	TYP	MAX	UNIT
Supply Voltage V _{CC} (See Note 1):								4.75	5	5.25	V
Fan-Out from Eoch Output	÷		٠							10	
Width of Clock Pulse t p(clock) (See Figure 9).	•	•	•	•	•	•	•	13	10		ns.
Setup Time Required at Serial, A, B, C, or D inputs t setup (See Figure 9)	÷							20	10		na
Hold Time Required at Serial, A, B, C, or D Inputs I hold (See Figure 9) .								0	-10		m
Logical 8 Level Setup Time Required at Mode Control † A(0)(See Figure 10) (With Respect to Clack 1 Input)								20			ns
Logical 1 Level Setup Time Required of Mode Control 18(1) (See Figure 10). (With Respect to Clock 2 Input)								15			ns .
Logical 0 Level Setup Time Required at Mode Control t _{C(0)} (See Figure 10) (With Respect to Clock 2 Input)								10			nı
Lagical 1 Level Setup Time Required at Made Control 1 _{D(1)} (See Figure 10) (With Respect to Clack 1 Input)								10			M

NOTES: 1. Valtage values are with respect to network ground terminal.

2. Input voltages must be zero or positive with respect to network ground terminal.

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS +	MIN	TYP	MAX	UNIT
Y _{In(1)}	Input voltage required to ensure logical 1 at any input terminal	1 and 3	V _{CC} = MIN	2			٧
V _{In (0)}	Input valtage required to ensure logical 0 at any input terminal	2 and 4	VCC = MIN			0.8	٧
V _{out (1)}	Lagical Lautput valtage	I and 3	V _{CC} = MIN, I _{lood} = -100 μA	2.4			٧
V _{out} (0)	Logical 0 output valtage	2 and 4	V _{CC} = MIN ₊ I _{slok} = 16 mA			0.4	٧
I _{In(0)}	Lagical 0 level input current at any input except made control	5	V _{CC} = MAX, V _{In} = 0.4 V			-1,6	mA
In(0)	Lagical O level Input current at mode control	5	V _{CC} = MAX, V _{In} = 0.4 V			-3.2	mΑ
I _{In(1)}	Logical 1 level input current at any input except mode control	6	V _{CC} = MAX, V _{In} = 2.4 V V _{CC} = MAX, V _{In} = 5.5 V			40	μA mA
I _{In(1)}	Logical 1 level input current at	6	V _{CC} = MAX, V _{In} = 2,4 V			ВО	μА
,.,	mode control		V _{CC} = AUX, V _{in} = 5.5 V			1	mA
los	Short-circuit output current	7	Y _{CC} = MAX	-18		-57	mA
^l cc	Supply current	8	VCC - MAX		50 F	85	mΑ

[†] For conditions shown as MtN or MAX use the appropriate value specified under recommended operating conditions. If Not more than one output should be shorted at a time. ‡ This typical value is at $V_{CC} = 5 \text{ V}$, $T_{A} = 25 \text{ °C}$.

switching characteristics, VCC = 5 V, TA = 25°C, N = 10

	PARAMETER	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
F max	PAssilmom shift frequency	9	C _L = 15 pF, R _L = 400 Ω	20	31		MHz
l _{pd1}	fropagation delay time to logical I level from clock I ar clock 2 to outputs	9	C _L = 15 pF, R _L = 400 Ω		26	35	796
†pd0	Propagation delay time to logical 0 level from clock 1 or clock 2 to output	9	C ₁ = 15 pF, R _L = 400 Ω		24	35	INS.

THE FOXBORO COMPANY SYSTEMS DIVISION

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A	LOCAL RELEASE PERECN 1917.			

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	OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11_	12	13	14	15	16
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	INTERCHANGEABLE SIMILAR TO		LOCAL RELEASE /				11/63	A			>		$\sqrt{3}$	300	28	, F	<u> </u>	
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FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package) 5-Bit Shift Register

- 2. PHYSICAL CHARACTERISTICS
 - 2.1 See Sheet 3.
- 3. PERFORMANCE CHARACTERISTICS
 - 3.1 See Sheet 6.
- 4. MANUFACTURER'S NAME AND PART NO.

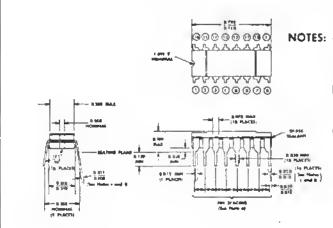
Texas Instrument, Part No. SN7496N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE SYMBOLI DRAWING NO.

A B V3008FS A

SCALE: SHEET 40F



- NOTES: a. The true-position pin spacing is 0.100 between centeilines. Each pin centeiline is located within ±0.010 of its true longitudinal position relative to pins (1)
 - b. All dimensions in inches unless otherwise noted.
 - c. This dimension does not apply for solder-dipped leads.
 - d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

16-PIN FUNCTIONS

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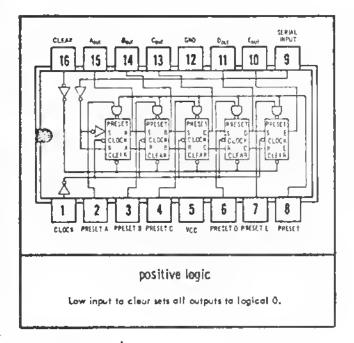
description

The SN7496N consists of five R-S master-slave flip-flops connected as a shift register to perform perallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/perallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flaps may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flap and the cammon preset input. The common preset input is provided to allow flaxibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input.

Transfer of information to the autput pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-5 master-slave circuits, the proper information must appear at the R-5 inputs of each flip-flap prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flaps provide information for the remaining R-5 inputs. The clear input must be at a logical 1 and the preset input must be at a logical 2 ond the preset input must be at a logical 2 ond the preset input must be at a logical 2 ond the preset input must be at a logical 2 ond the preset input must be at a logical 3.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Valtage V _{CC} (See Note 1)	٠	٠	٠	٠	٠	٠	٠	٠	٠	٠	٠	٠	•	٠	٠	٠	•		٠		٠	•	. 7	٧
Input Valtage V _{in} (See Nates 1 and 2)	٠	٠		٠		٠	٠	٠	٠	•	•				٠		٠				٠	٠	5.5	٧
Operating Free-Air Temperature Range																					(0°C	ta 70°	*C
Storage Temperature Range		٠				٠	٠		٠		٠		٠			٠		٠	•	-	55°	'C to	1 150	,C

NOTES: 1. These valtage values are with respect to network ground terminal.

2. Input signals must be zera or positive with respect to network ground terminal.

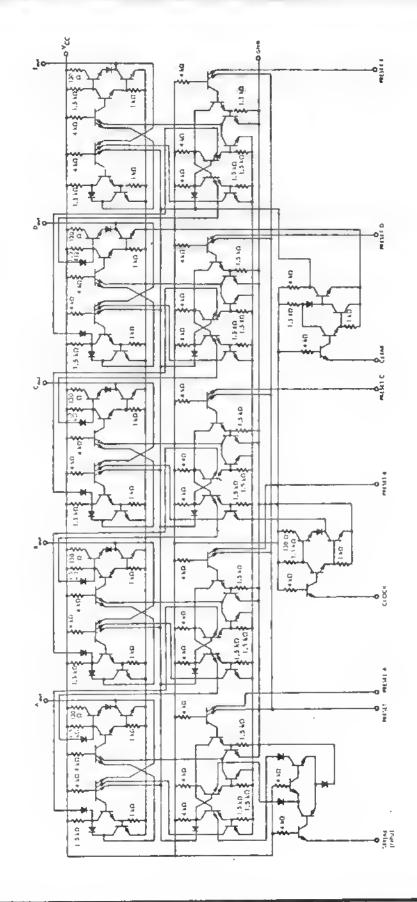
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Sheet 5 of

Supply Valtage Van (See Note 1	١.															MIN	TYP	MAX	UNIT
Supply Valtage V _{CC} (See Note)	···	*	*	•						٠						4.75	. 5	5.25	V
																		10	
Width of Clock Pulse, t p(clock)			•	•	•	•	•		•	•	•	•		•	•	35			ns.
p(clear)																30			Dil
D(oreset)																30			ns.
Serial Input Setup Time, t																30			114
Serial input Hold lime, thoid									•	•	•		•	•	•				715
NOTE Is This value on the in-			•	•	•		•	•	a	•	*					0			F1.9

NOTE 1: This valtage value is with respect to network ground terminal. electrical characteristics (over operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{In(1)}	Input voltage medited to ensure logical 1 at any Input terminal	VCC # MIN	2			V
V _{Jn(0)}	Input voltage required to ensure logical 0 at any input terminal	Y _{CC} = MIN			0.8	V
V _{out(1)}	Logical 1 output voltage	V _{CC} = MIN _s I _{load} = -400 μA	2,4	3.5		V
V _{out} (0)	Logical O output valtage	VCC = MIN, I sink = 16 mA		0.22	0.4	V
I _{In(1)}	Logical 1 level input current at any input except	V _{CC} = MAX + V _{In} = 2.4 V			40	μA
	Preset (pln (8)	V _{CC} = MAX, V _{In} = 5.5 V			+1	mА
l In(1)	Logical 1 level Input current at Preset (pin (8))	V _{CC} = MAX = V _{In} = 2,4 V			200	μA
	contain of (least (pin (g))	V _{CC} = MAX, V _{In} = 5.5 V			1	mA
ln(0)	Logical O level input current at any input except Preset (pin (3))	V _{CC} = MAX, V _{In} = 0.4 V			-1.6	mA
In(0)	Logical O lavel Input current at Preset (pin (5))	V _{CC} = MAX, V _{In} = 0.4 V			-B	mA
os	Short-circuit autput	V _{CC} = MAX, V _{out} × 0	-18		-57	mA
CC	Supply current	V _{CC} = MAX		48‡	79	mA

[†] For conditions shawn as MIN or MAX, use the appropriate value specified under recommended operating conditions. † Those typical values are at $V_{CC} = 5$ V and $T_A = 25^{\circ}$ C.

switching characteristics, V_{GC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
max	Maximum clock frequency	C _L = 15 pF, R _L = 400 Ω	10			MHz
[†] pd1	Propagation delay time ta logical 1 level from clock ta output	C _L = 15 pF, R _L = 400 Ω		25	40	Z1:S
† _{pd} 0	Propagation datay time to fection 0 level from clack to cutput	C _L = 15 pF, R _L = 400 Ω		25	40	ns
¹ pd1	Proposition delay time to logical Llevel from preset to autout	C _L = 15 pF, R _L = 400 Ω			35	ns.
t _{pd0}	Propagation Catay time to logical Ollevel from present to output	C _L = 15 pF, R _L = 400 Ω			40	HE

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⁹ Not more than one output should be shorted at a time.

